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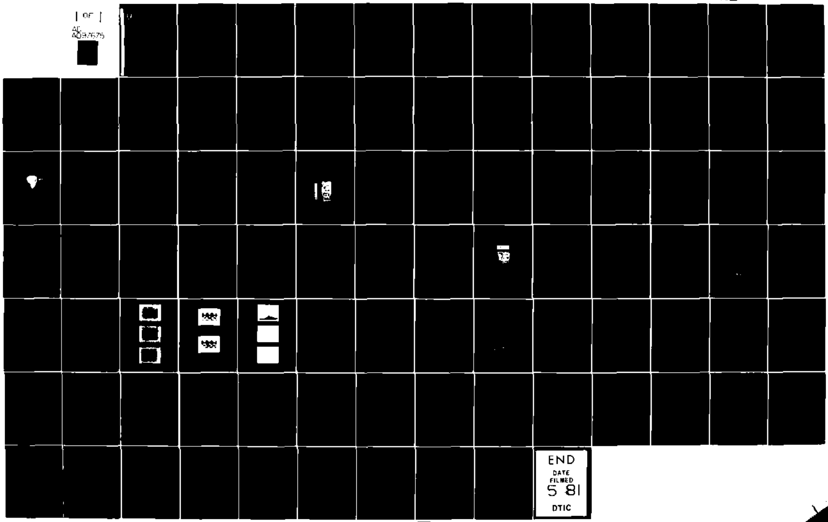

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Research and Development Technical Report

DELET-TR-80-0260-1

AD A097 075

403 MHz SAW OSCILLATOR

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This contract provides for a twelve (12) month program for the investigation and exploratory development of a 200 mW, SAW stabilized oscillator which can be frequency and amplitude modulated. The oscillator is to have its center frequency at 403 MHz and be tunable over a + 3 MHz bandwidth. Trade-off design studies have been performed to determine techniques which will provide the most effective interaction of essential oscillator components, i.e., SAW delay-line, phase shifter, coupler and amplifier, to provide a high degree of frequency stability. A significant effort was made to implement the required

circuit functions in a low-cost printed circuit approach rather than utilize high-cost commercially available components, since the oscillator is intended for use in an expendable application.

Specific tasks addressed to date include: Mask and SAW delay line design and fabrication. Assembly of a DC circuit board as required for electronic tuning, modulation, compensation and regulation. Integration and test of a complete breadboard oscillator. Extensive circuit characterization.

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1. SUMMARY

The objective of this program is the development of a 403 MHz surface acoustic wave oscillator suitable for use in an expendable radiosonde. Due to the extreme temperature range (-70°C to +70°C) the radiosonde must operate in and the simultaneous deployment of many radiosondes operating within a limited bandwidth, temperature stability is the oscillator's most critical performance parameter. Stability of 200 ppm or better is required. The circuit is also required to tune from 400 MHz to 406 MHz, transmit 200 mW (+23 dBm), and be capable of both amplitude and frequency modulation. Specified performance is outlined in Table 1-1.

Table 1-1. Oscillator Performance Specifications

Parameter	Specification	Comment
Frequency	400-406 MHz	Settable to 50 ppm
Stability	200 ppm	-70°C to +70°C
Modulation		
PAM	0 to 2000 pps	
FM	100 KHz Modulation Frequency	300 KHz/V Modulation Sensitivity
Output Power	200 mW	50 ohm load
Frequency Pulling	$\leq \pm 20$ ppm	Z_L = 25 to 75 ohms
Power Supply	24V $\pm$10% <2.5 watts	Other supply voltages can be considered

During the first six months of the program the oscillator design has been completed, and all the individual RF subcircuits have been designed, fabricated and tested. These circuits include the SAW delay line, loop amplifier, phase shifter, and an injection locked oscillator. This report discusses overall

oscillator design, and gives a detailed description of the design and performance of the various subcircuits of the oscillator. The oscillator design is described in Section 2, while the design and performance of the individual subcircuits are described in Section 3. Measured performance not found in Section 3 can be found in the Appendix.

2. OSCILLATOR DESIGN

A block diagram of the 403 MHz SAW Stabilized Oscillator is shown in Figure 2-1. The circuit consists of a relatively low power, tunable SAW oscillator driving an injection locked oscillator, plus associated DC circuitry. The SAW oscillator produces approximately 20 mW (+13 dBm) RF power, tunable from 400 MHz to 406 MHz. Both mechanical tuning for frequency selection and electronic tuning for frequency modulation are employed. The injection locked oscillator which is locked to the SAW oscillator output produces an RF output in excess of 200 mW (+23 dBm). The ILO therefore provides approximately 10 dB of gain. Bias switching circuity in the ILO is used for pulse amplitude modulation (PAM). The DC circuitry (not yet designed) will consist of a voltage regulator to minimize frequency pushing, tuning and frequency modulation circuitry, and a temperature compensation network to compensate for both varactor reactance changes and SAW delay variation with temperature.

The heart of this circuit is clearly the SAW oscillator. The conditions for oscillation in this circuit are (1) gain around the loop must exceed all losses and (2) phase around the loop must equal a multiple of 2π radians. These conditions can be expressed as

$$L_S(f) + L_I(f) \le G(f,A) \tag{2.1}$$

and

$$\frac{2\pi f_N \ell}{V} + \phi = 2N\pi \tag{2.2}$$

where

f_N = oscillation frequencies

; = center-to-center transducer separation

V = surface wave velocity

: = phase shift through all elements except SAW delay line

N = an integer

$L_S(f)$ = insertion loss of SAW delay line

$L_I(f)$ = insertion loss of feedback loop components

G(f,A) = amplifier gain as a function of and output level, A

A = output power level

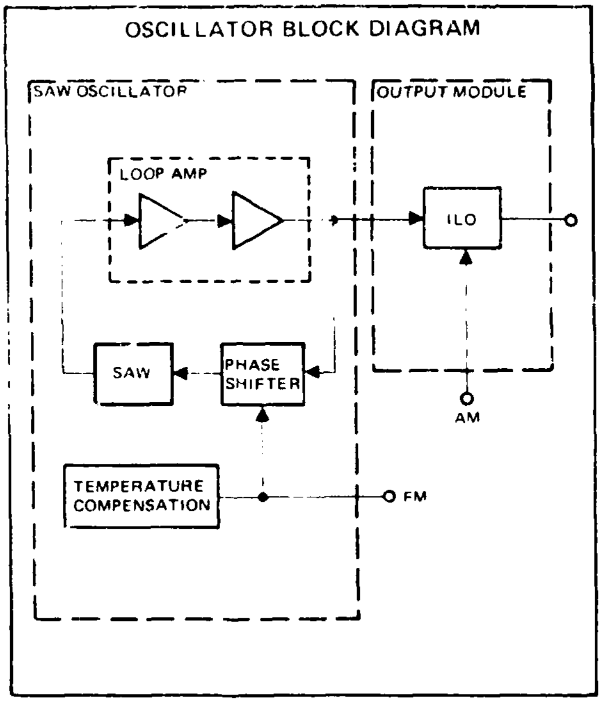

Figure 2-1. Oscillator Block Diagram

The frequency of oscillation can be determined from equation (2.2)

$$f_N = \frac{V}{\ell} \left(N - \frac{\phi}{2\pi}\right) \qquad (2.3)$$

It is possible for multiple solutions to equations (2.1) and (2.2) to exist as shown in Figure 2-2 where many solutions to the phase condition exist within the SAW passband. For single-mode operation, the SAW delay line is designed such that there is only one solution for equation (2.2) which is in the passband of the delay line. Such a design is shown in Figure 2-3. As a general rule, the loss associated with the feedback loop components, $L_I(f)$, and the amplifier gain, $G(f,A)$, are slowly varying functions of frequency over a broad range around the frequency for which the oscillator is being designed, and the SAW response, $L_S(f)$, is a very strong function of frequency. The SAW oscillator is designed so that the combination of SAW delay line loss plus amplifier gain exceeds unity over a desired frequency band around the desired operating frequency. As long as only one solution to (2.2) falls within the passband response of the SAW delay line, single mode operation of the SAW oscillator is guaranteed.

The loop amplifier shown in Figure 2-4 provides gain to overcome losses around the loop - thereby meeting the first condition for oscillation (equation (2.1)). The amplifier is designed to have linear gain well in excess of the loop losses. The required gain margin is a function of the saturation characteristics of the amplifier chain, but typically must be greater than 4 dB. Measurements made at TRW have shown that a minimum of 4 dB gain margin will provide maximum output power and minimum phase noise. The effect of gain margin on oscillator output power and phase noise is shown in Figures 2-5 through 2-8. For a circuit with adequate gain margin, the oscillator output power will equal the saturated output power of the amplifier minus the power coupled back into the loop.

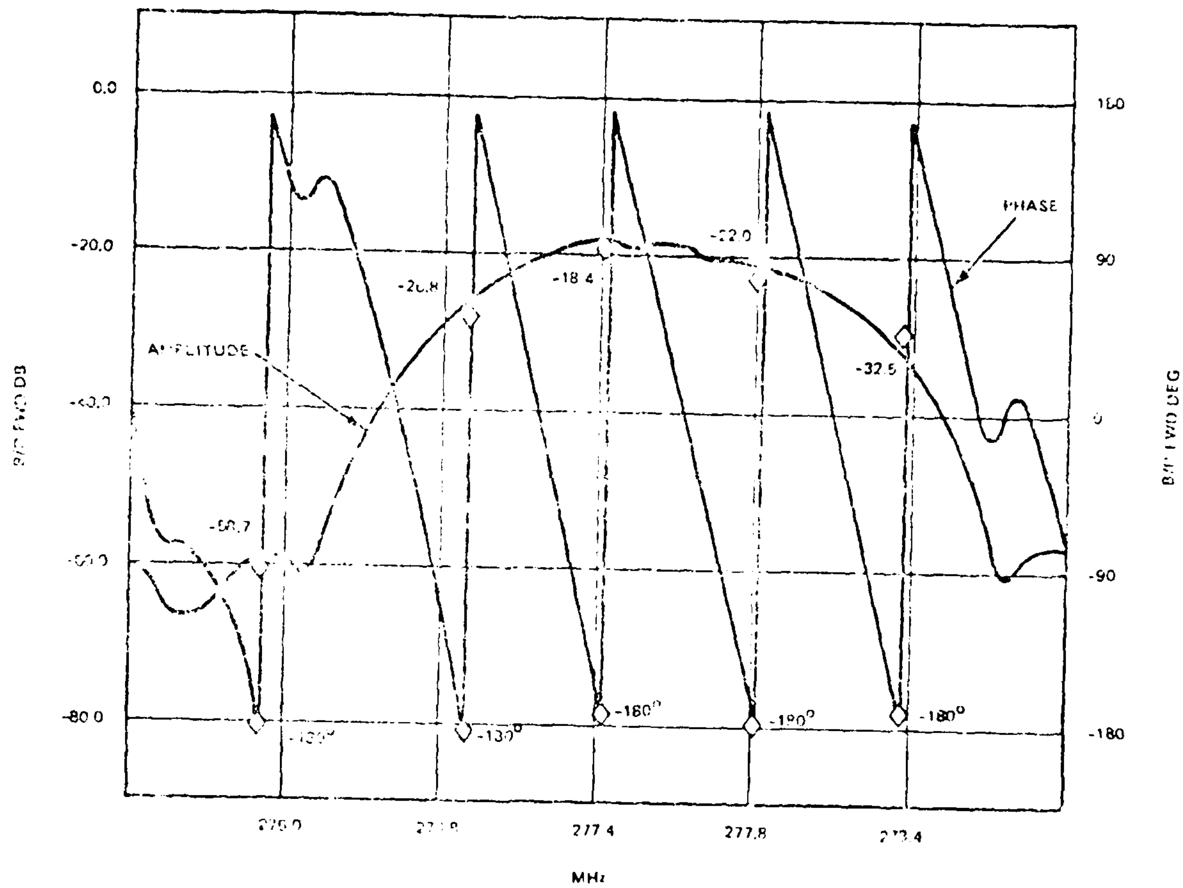

Figure 2-2. SAW Delay Line: Multiple Modes

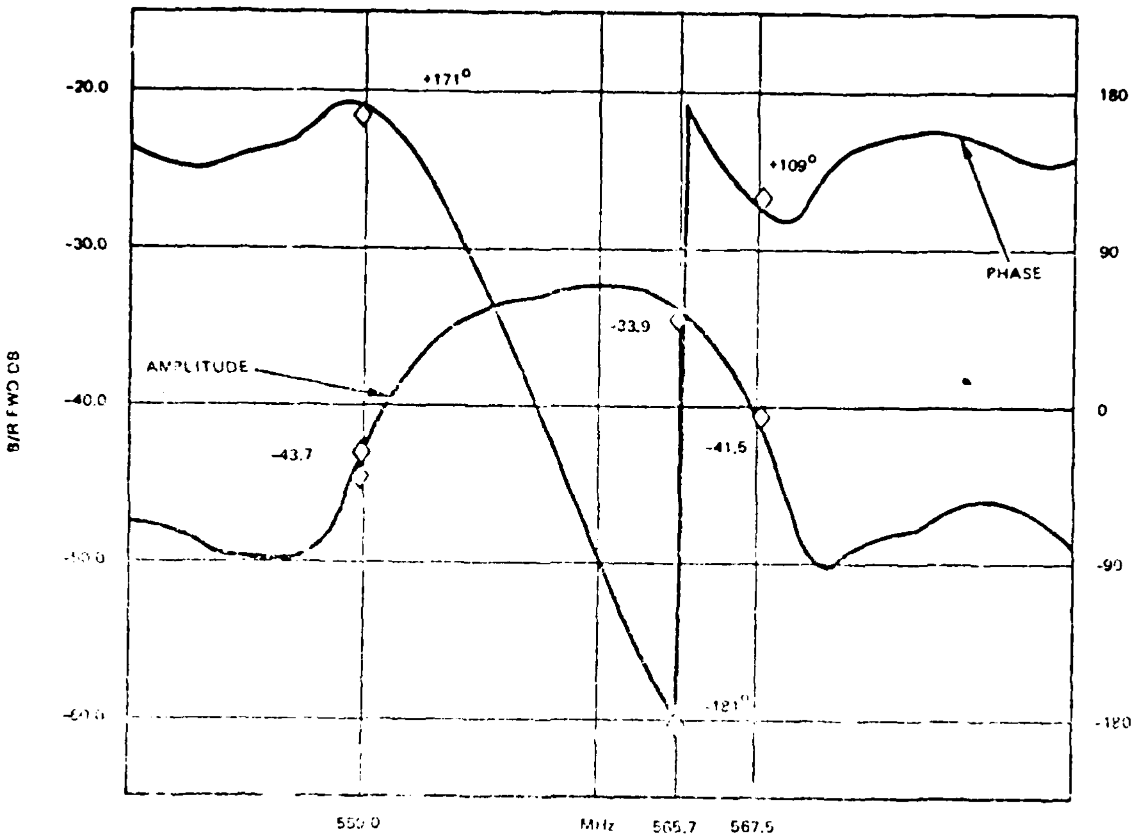

Figure 2-3. SAW DELAY LINE: SINGLE MODE

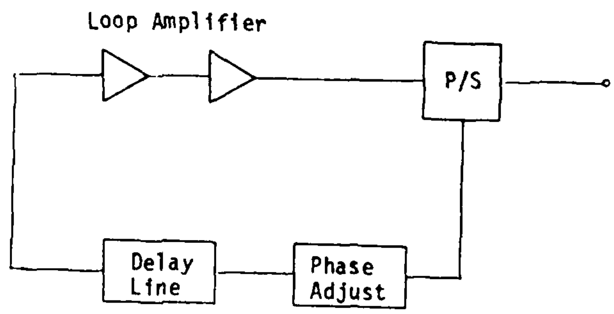

Figure 2-4. SAW DELAY LINE OSCILLATOR

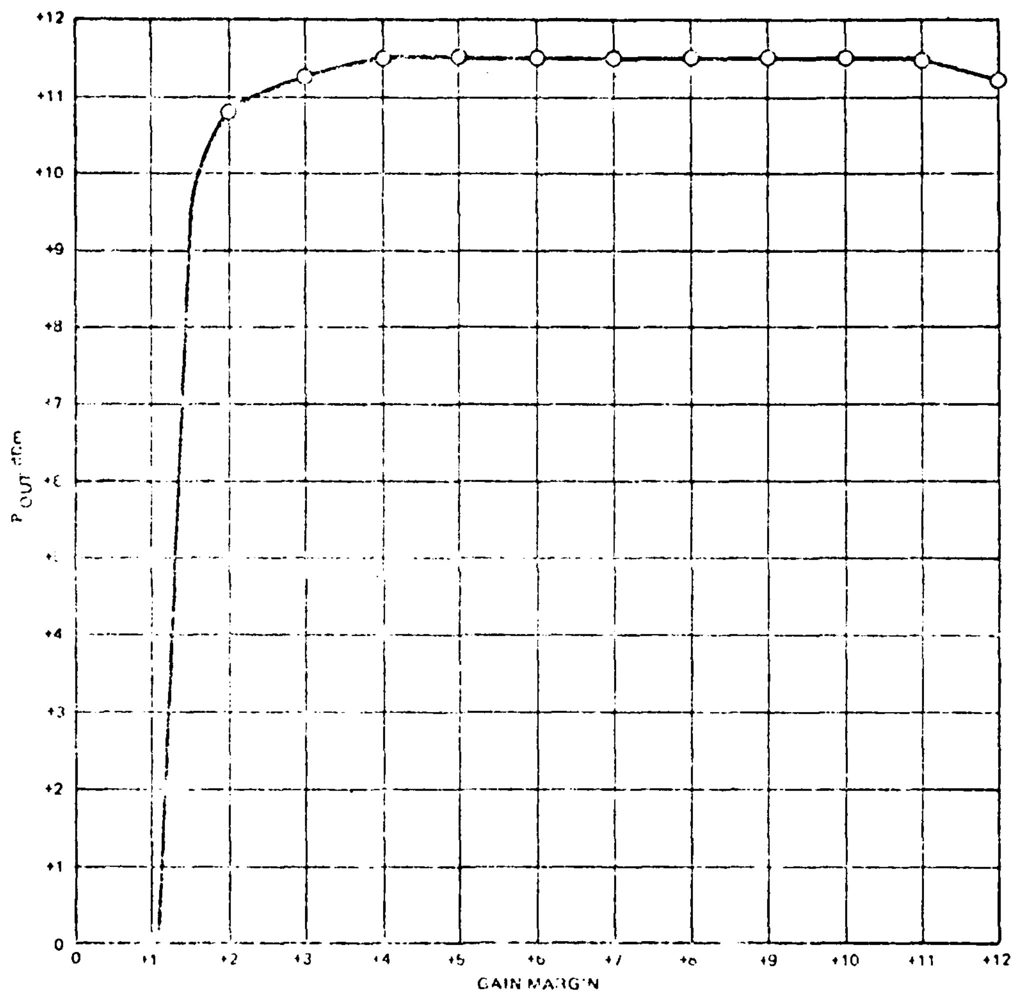

Figure 2-5. Output Power vs Gain Margin

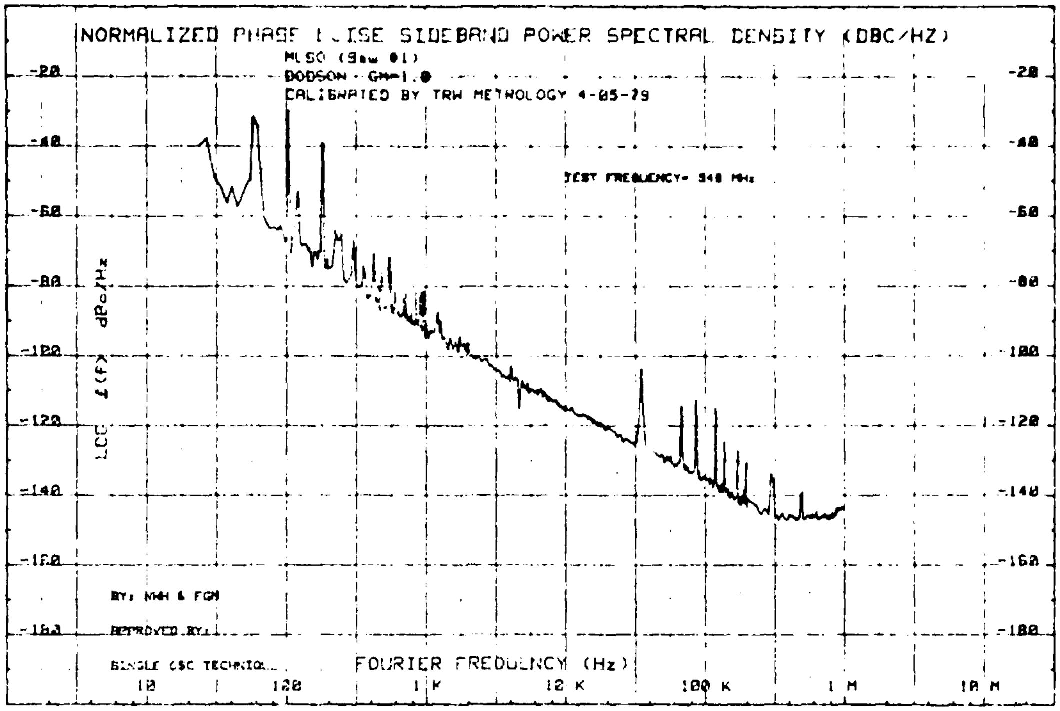

Figure 2-6. Oscillator Phase Noise for Gain Margin of 1 dB

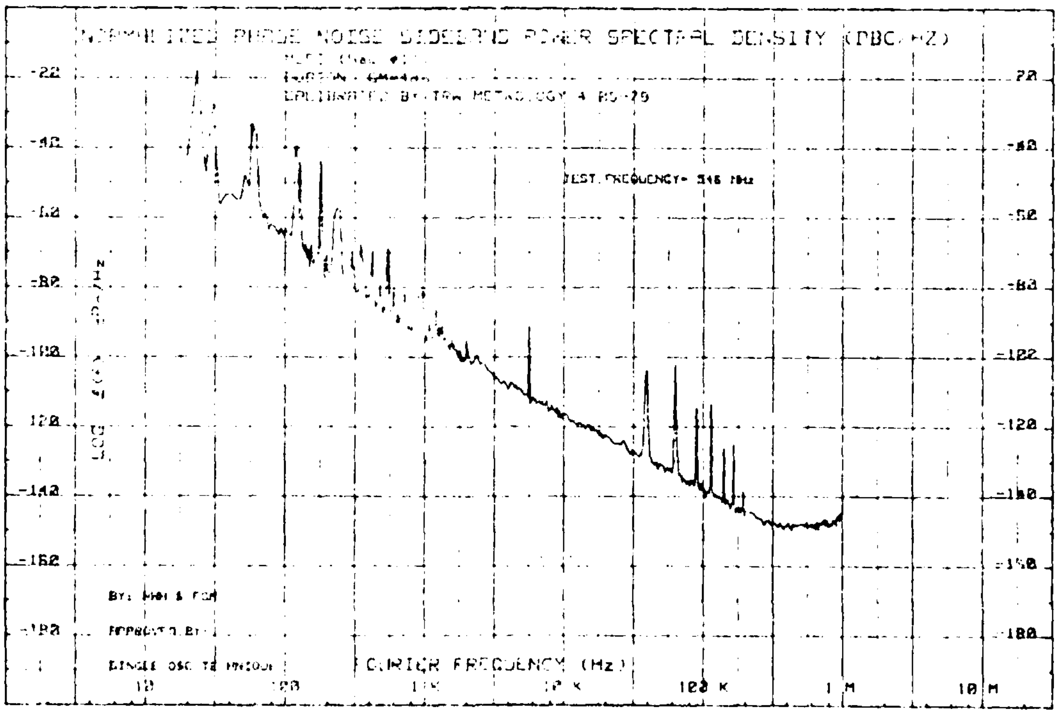

Figure 2-7. Oscillator Phase Noise for Gain Margin of 4 dB

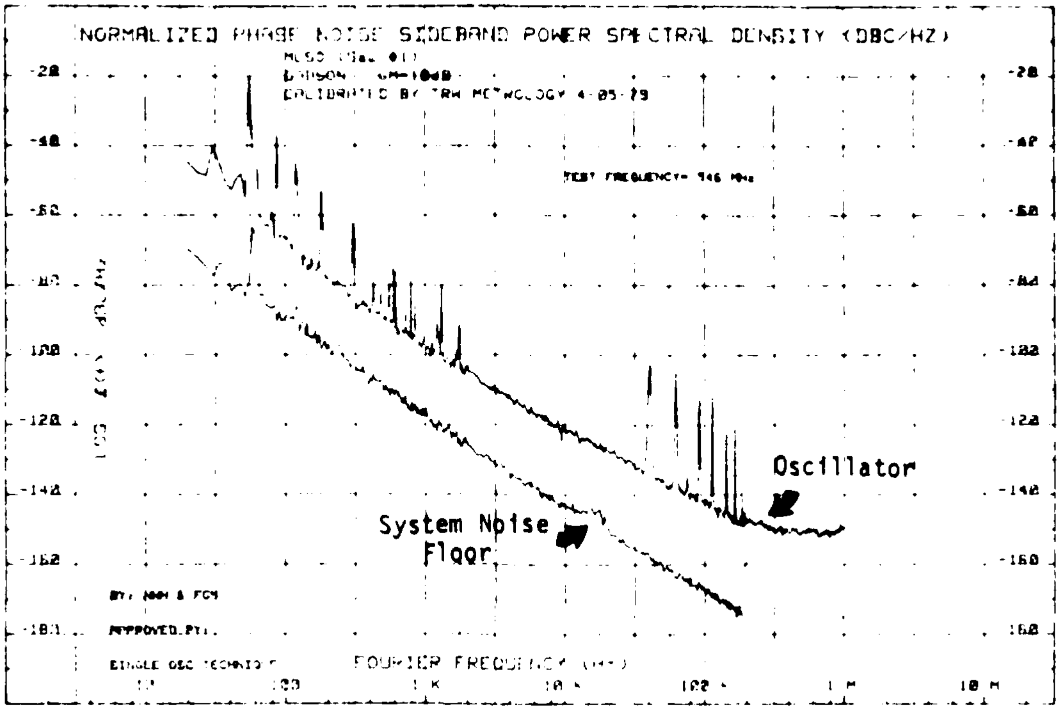

Figure 2-8. Oscillator Phase Noise for Gain Margin of 10 dB

The second condition for oscillation, equation (2.2), is met through use of the phase shifter shown in Figure 2-4. The frequency of oscillation is set by varying : in (2.3). It is necessary for the phase shifter to provide adequate phase variation to tune across the required frequency band. This phase variation will be defined by the phase slope of the delay line. It is generally necessary to provide tuning phase in excess of that required for any given SAW to accomodate the variation in absolute transmission phase from SAW to SAW. It is reasonable to expect variations in absolute delays for SAWs to be as large as +0.1%. For typical delay lines of 100λ electrical length, this equates to $\pm 36°$ variation in transmission phase. The data from measurements of 16 delay lines shown in Table 2-1 demonstrates typical variation in absolute phase. It is often required that a full 360° of phase shift be provided to accomodate tuning range and variation from SAW to SAW.

Table 2-1. MEASURED VARIATIONS IN ABSOLUTE PHASE

[illegible] DESIGNATION	DESIGN FREQUENCY	TRANSMISSION PHASE	MAXIMUM PHASE DIFFERENCE
B1 1 B2 1 [illegible] B[illegible]	555.0 MHz	76.5 112.5 119.0 80.0	36°
B1 [illegible] [illegible] 2 [illegible] [illegible] 4 2	[illegible]	128.0 [illegible] 6 145.[illegible] 16[illegible] 0	59.4°
[illegible] 1 [illegible] B2 [illegible] [illegible] [illegible] 1 3	[illegible]	10[illegible] 0 +[illegible] 5 +9[illegible] +[illegible] 0	40°
B1 [illegible] [illegible] 4 B3 4 B4 [illegible]	[illegible]	157.5 144.0 98.0 +155.0	107°

Based on these general considerations, specifications for the individual oscillator subcircuits have been generated. These specifications are shown in Table 2-2.

Table 2-2. OSCILLATOR SPECIFICATIONS

Circuit	Parameter	Specified Performance	Comments
Delay Line	Center Frequency	403 ±0.150 MHz	ST-cut quartz
	3 dB Bandwidth	6.3 MHz	
	Loss (Matched)	≤ 20 dB	
	Delay	~100 ns	
Loop Amp	Frequency Band	>350-450 MHz	
	Gain	≥ 40 dB	
	P_{SAT}	≥ 16.5 dBm	
	VSWR (In,Out)	≤ 2.5:1	
	V_{Supply}	12V	
Phase Shifter	Loss	<3 dB	Two cascaded phase shifters to be used
	Phase Shift	≥180°	
	Tuning Voltage	1-10V	
Power Splitter	Coupling	3.0 dB	
	Loss	≤0.5 dB	
ILO	Natural Frequency	403 MHz	
	Power Out	≥ +23 dBm	200 mW
	Injection Locking Bandwidth	±16 MHz	Greater locking range may be required to accomodate temperature effects
	P_{IN_j}	+13 dBm	
	V_{Supply}	12V	

As these specifications imply, a 12V supply will be used throughout. All of the transistor circuitry would perform optimally with a 12V supply. Only the varactors in the phase shifter would benefit from using the full 24V available and due to the varactor C-V relationship, this benefit is small. The 12V supply was therefore chosen to conserve power.

A review of Table 2-1 points out key features of the design. The loop amplifier gain of 40 dB exceeds the 30 dB loop loss by 10 dB. This is adequate to drive the amplifier well into saturation and provides margin for SAW and phase shifter variations. The delay in the SAW implies a mode spacing of 1.0 MHz. If 20 ns of delay in other components in the loop is assumed the mode spacing would be reduced to 8.3 MHz. This is well in excess of the 7 MHz 3 dB bandwidth of the SAW. Two phase shifters will be used in cascade. A single phase shifter (of the design contemplated) will produce no more than 250° phase shift. Therefore, two are required to produce a 360° phase shift. The ILO will lock over a range far in excess of the 6 MHz operating band. This is to account primarily for the drift in ILO natural frequency with temperature.

In the following section the design and performance of these individual circuits is discussed in detail.

3. CIRCUIT DESIGN AND PERFORMANCE

a. 403 MHz SAW Delay Line

It is required that the 403 MHz SAW oscillator be operated with one stable single mode output and be tunable over the 400 MHz to 406 MHz frequency range. To achieve this, the specifications for the SAW delay line were set as follows:

Center Frequency	403.0 $\pm$0.15 MHz
3 dB Bandwidth	6.3 $\pm$0.1 MHz
Time Delay	0.10 $\pm$0.01 μsec
Insertion Loss (matched)	< 20 dB
Substrate	ST Quartz
Temperature Stability	
Turnover Temperature (T_0)	$-10°C < T_0 < 10°C$
2nd Order Temperature Coefficient	$-3.2 \times 10^{-8}/(°C)^2$

The ST-cut of quartz was chosen because it is one of the most temperature stable SAW substrates available. Its turnover temperature (T_0) for the free surface condition is near 23°C. However, with metal loading (approximately 700 Å aluminum), T_0 is expected to be lowered near 0°C. The 3 dB bandwidth requirement is set so that in addition to covering the operating frequency range, there is a 0.2 MHz margin to allow for center frequency variation in the SAW device.

The most critical parameter in the SAW requirement is the time delay. In the present case, the time delay has been specified to be much shorter than that normally considered necessary for single mode operation. This is because the external time delay in the oscillator loop due to elements other than the SAW delay line can be a significant portion of the total delay. Preliminary results indicate that for the proposed SAW oscillator, external delay amount to at least 20 ns. This will increase the total loop delay to approximately 0.12 to 0.13 μsec. The mode spacing of the oscillator will thus be on the order of 7 MHz and not the 10 MHz which one would get if the external delay is neglected. With 7 MHz mode spacing, single mode operation can be achieved if the amplifier gain is set properly.

To meet these specifications, the delay line was designed to consist of one long and one short transducer, closely spaced one next to the other. The 3 dB bandwidth is largely defined by the long transducer. The transducers are both designed to operate at the fundamental frequency and contain split fingers to minimize reflection among fingers. The center-to-center separation between transducers in 40.3 λ_0, where λ_0 is the acoustic wavelength.

The other design parameters are shown in the following table:

	Input Transducer	Output Transducer
Number of Finger Paris	30	50
Acoustic Aperture	45 λ_o	45 λ_o
Finger Width	1.3 μm	1.3 μm

The unmatched insertion loss of such a device should be approximately 40 dB. Upon matching, it can be reduced to 18 dB or less.

The schematic of the SAW delay line is shown in Figure 3-1. A ground bar has been placed between the transducers to cut down the direct electrical feedthrough.

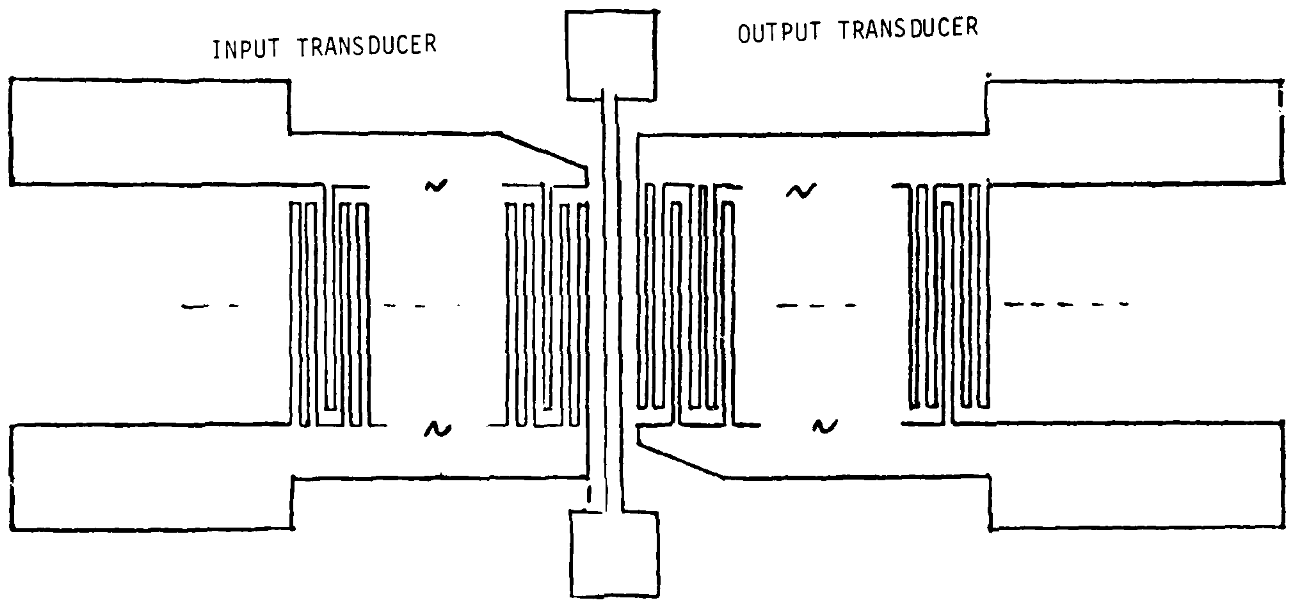

Figure 3-1. SCHEMATIC OF 403 MHz SAW DELAY LINE

This delay line has been designed, fabricated and tested. Performance of the unmatched delay line is shown in Figures 3-2 through 3-4. The circuit has been packaged in a TO-5 can to minimize size and cost. A photograph of the packaged SAW is shown in Figure 3-5. Matching networks for the SAW have also been designed, built, and tested. A schematic of the matched circuit is shown in Figure 3-6. Performance of the matched delay line is shown in Figures 3-7 and 3-8.

b. Loop Amplifier

The loop amplifier is used to provide gain to overcome losses in all other loop elements. A schematic of the amplifier used for the SAW oscillator is shown in Figure 3-9. The circuit is a three-stage, lumped element design using two BFR 91 transistors and one MRF 559. The MRF 559 is used in the amplifier output stage to provide saturated output power in excess of 40 mW (+16 dBm). A lumped element design was used to minimize circuit size. Distributed matching networks would have required more volume than available.

This circuit has been designed, built, and tested. A photograph of the breadboard circuit is shown in Figure 3-10. Test results for the amplifier are shown in Figures 3-11 through 3-16. Figure 3-11 shows linear gain in excess of 40 dB for temperatures ranging from -70°C to +70°C. Saturation characteristics for the circuit are shown in Figures 3-12 and 3-13. Saturated gain for input power of +18 dBm is shown in Figure 3-14. Transmission phase through the amplifier for inear and saturated operating conditions is shown in Figures 3-15 and 3-16, respectively.

All of the data shown above has also been taken as a function of supply voltage. Results indicate that the transmission phase of the amplifiers is sensitive to supply voltage particularly at temperature extremes. The supply to the amplifier will therefore be regulated to 9V.

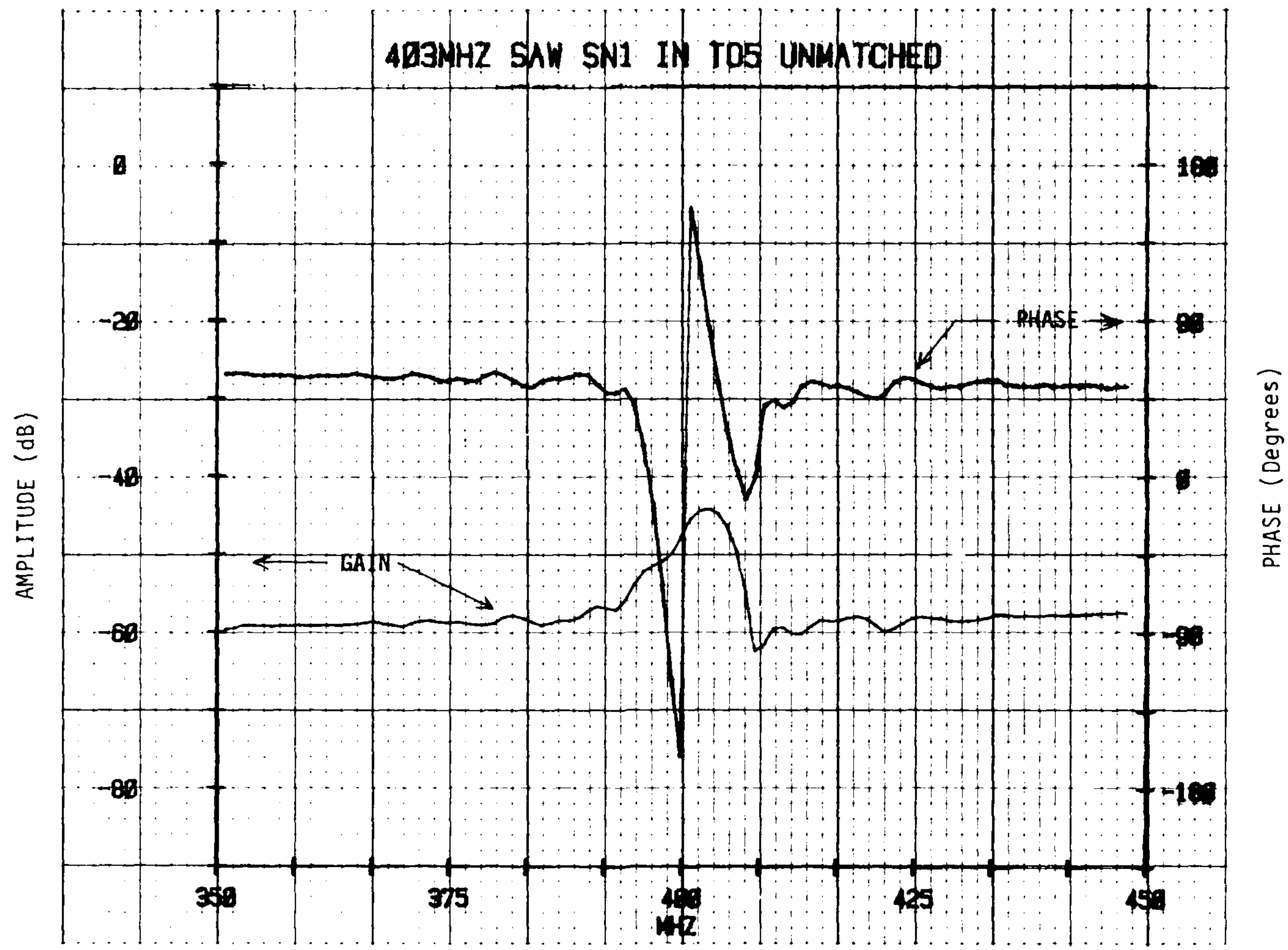

Figure 3-2. 403 MHz SAW Unmatched Passband and Phase

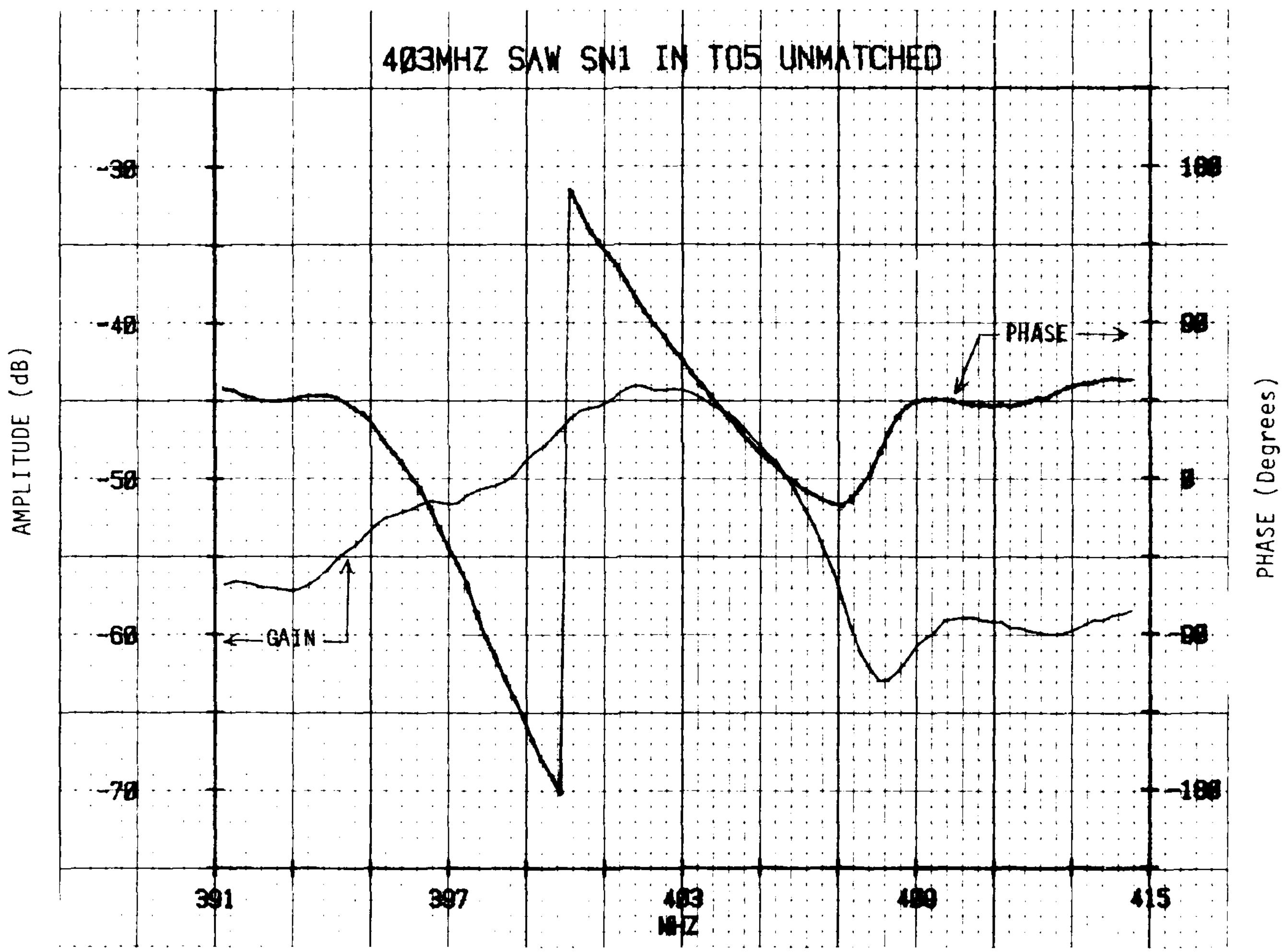

Figure 3-3. 403 MHz SAW Unmatched Passband and Phase

NAME 403 MHZ SAW SN1	TITLE IN T05	DWG. NO
SMITH CHART FORM 82-BSPR(9-66)	KAY ELECTRIC COMPANY PINE BROOK N.J. ©1966 PRINTED IN U.S.A.	DATE

IMPEDANCE OR ADMITTANCE COORDINATES

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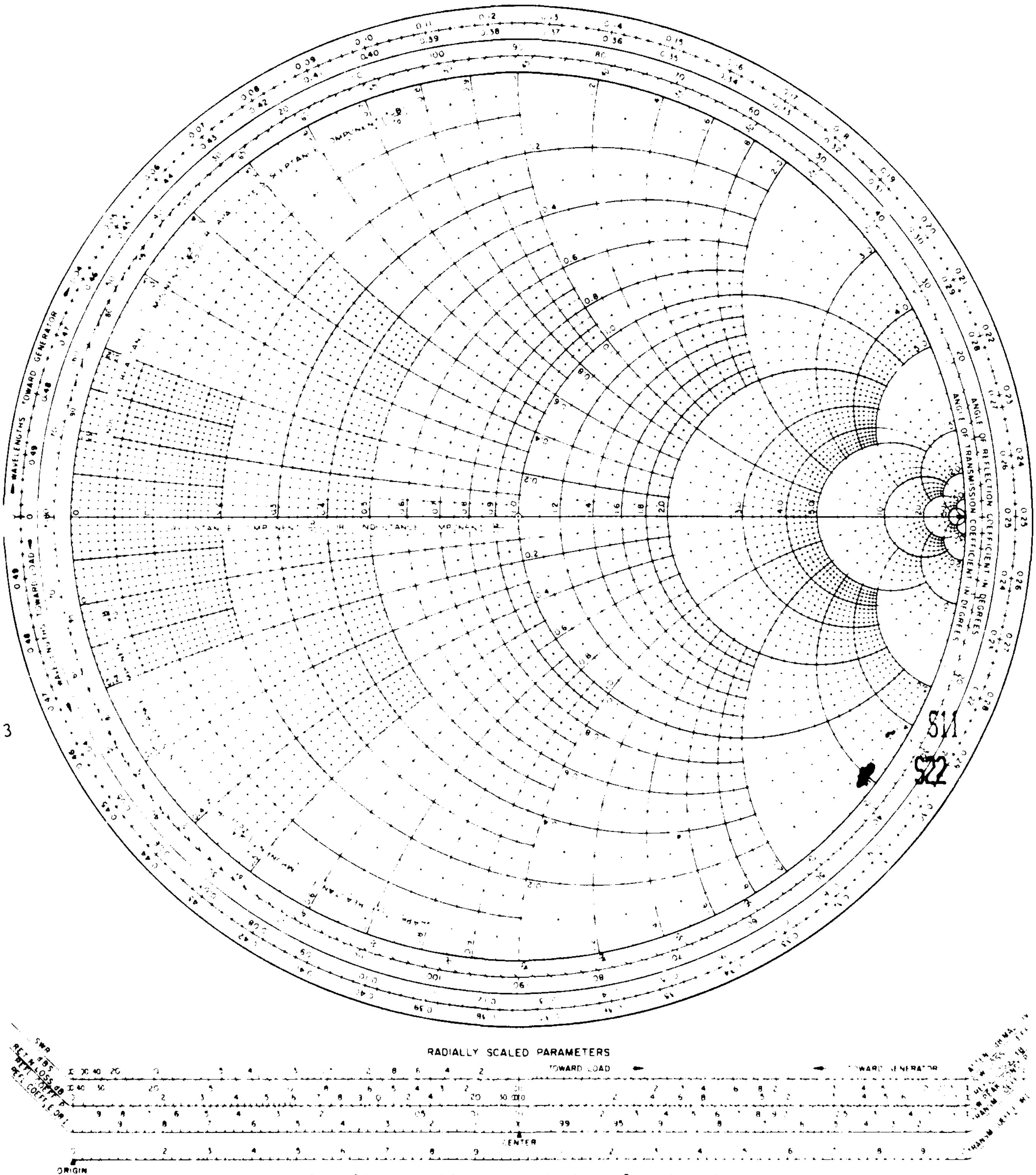

Figure 3-4. 403 MHz SAW Unmatched Reflection Coefficients

A MEGA-CHART

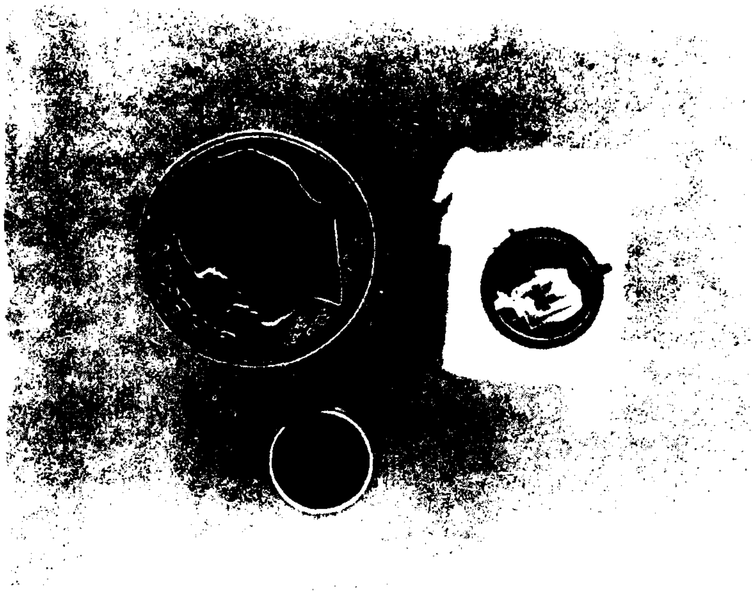

Figure 3-5. PHOTOGRAPH OF PACKAGED SAW

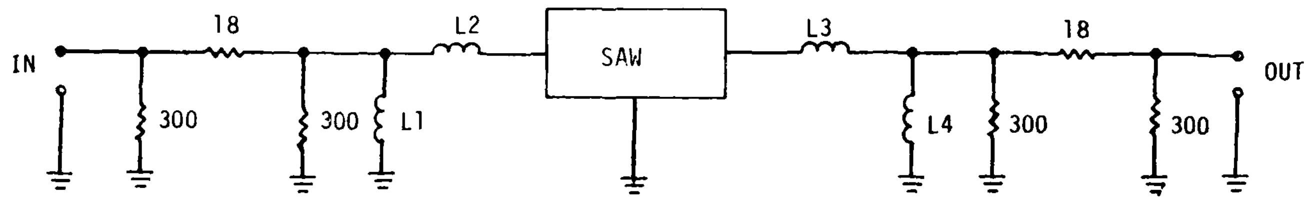

Figure 3-6. 403 MHz SAW DELAY LINE

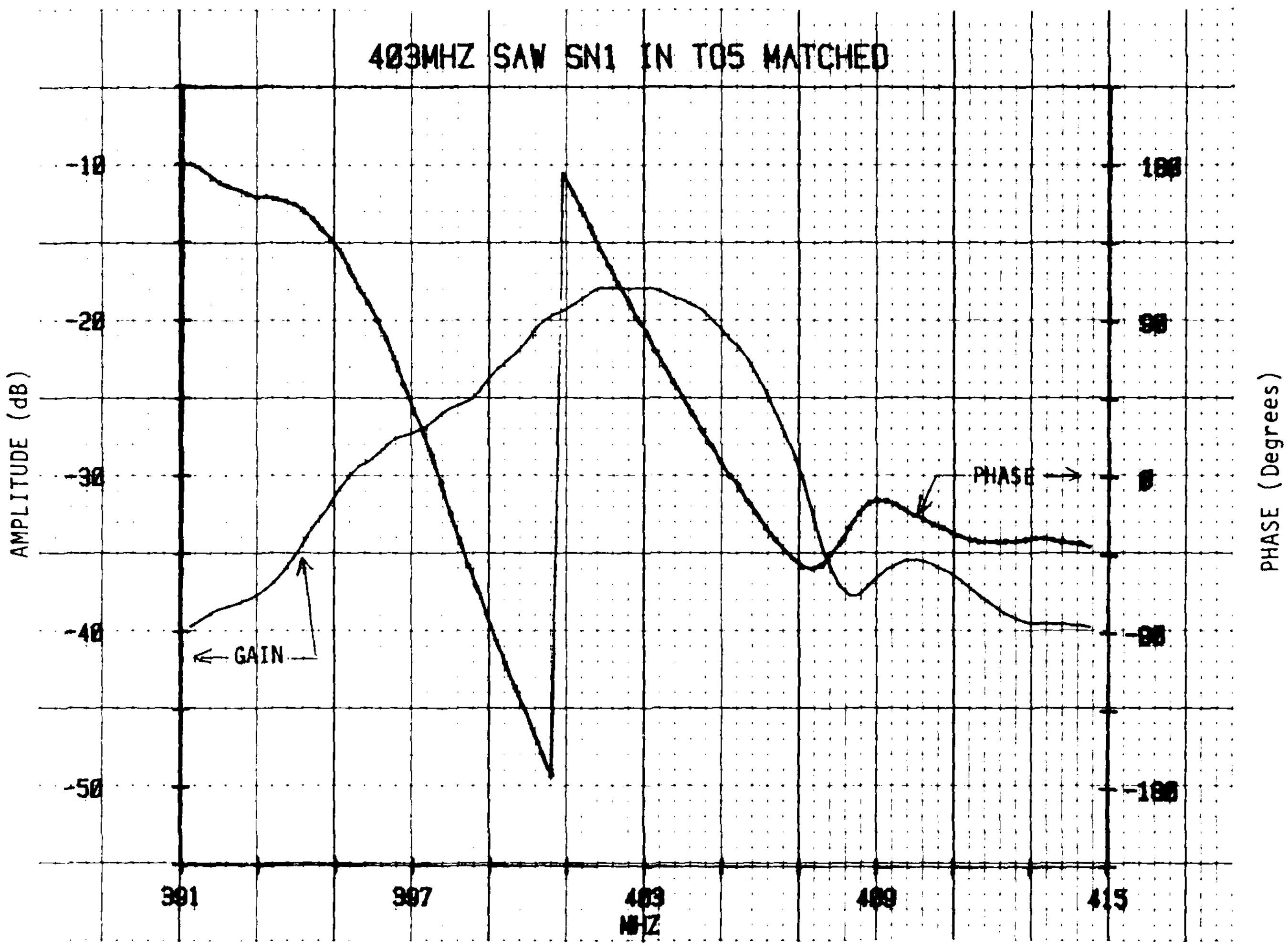

Figure 3-7. 403 MHz SAW Matched Passband and Phase

NAME 403 MHZ SAW SN1	TITLE IN T05 MATCHED	DWG. NO
SMITH CHART FORM 82-BSPR(9-66)	KAY ELECTRIC COMPANY PINE BROOK N.J. ©1966 PRINTED IN U.S.A.	DATE

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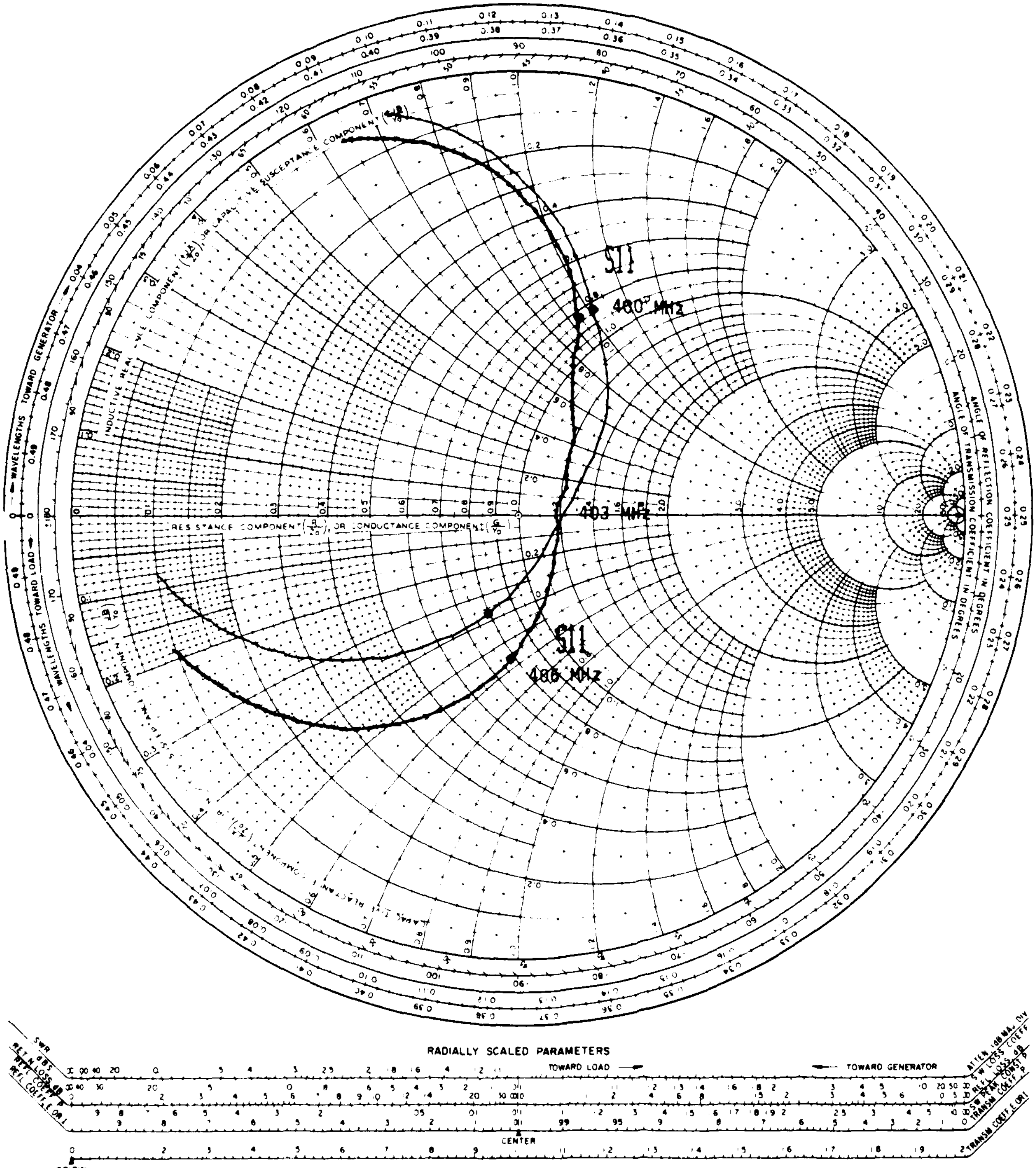
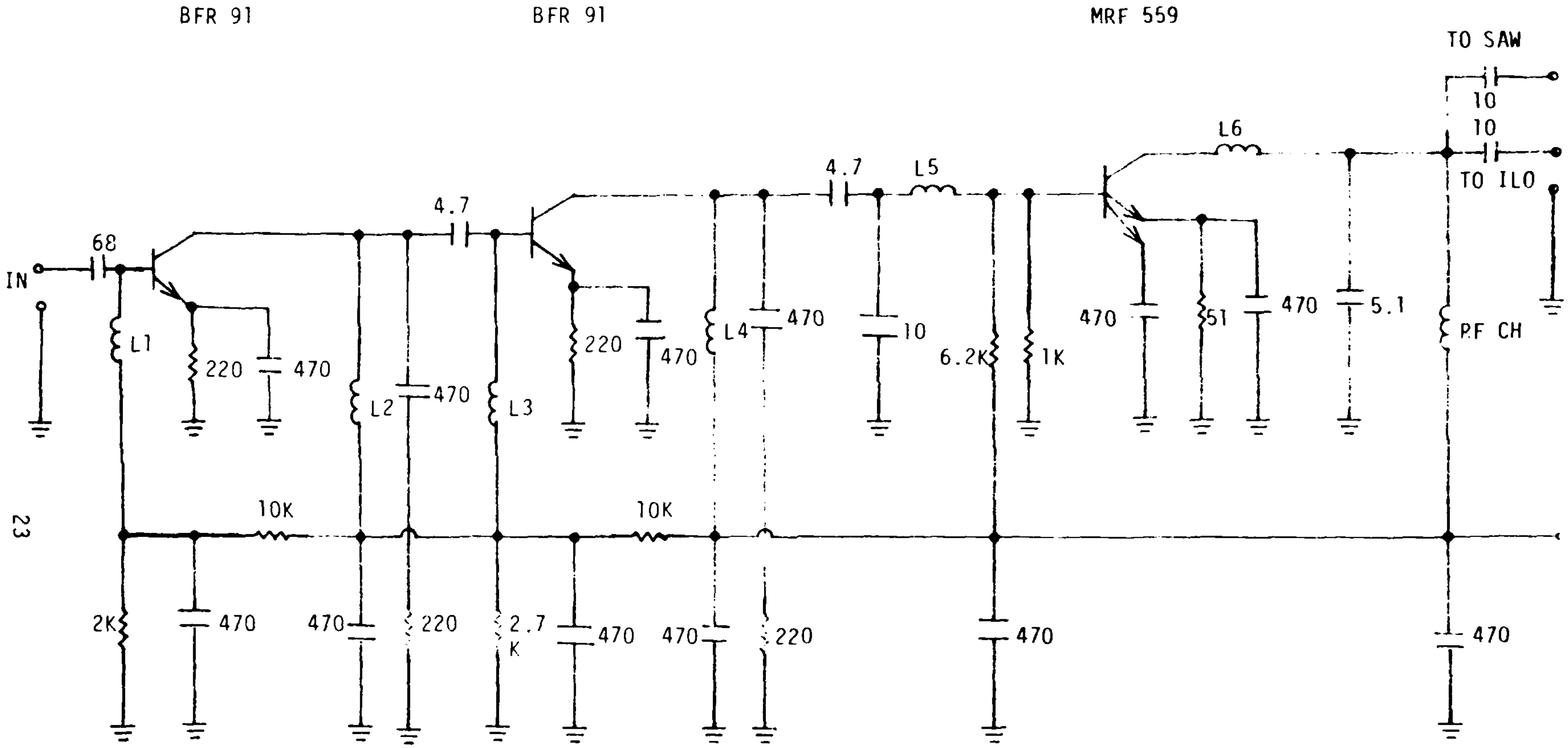


Figure 3-8. 403 MHz SAW Matched Reflection Coefficients

A MEGA-CHART



L1 = L3 = 5 turns #30 wire on #60 drill.

L2 = L4 = 6 turns #30 wire on #60 drill.

L5 = 3 turns #30 wire on #60 drill.

L6 = 11 turns #30 wire on #60 drill.

RF CH = 0.5 μH inductor.

Figure 3-9. 403 MHz SAW AMP

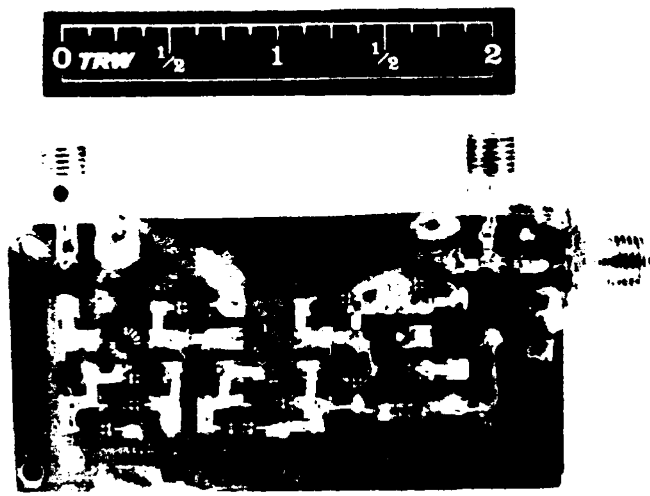


Figure 3-10. PHOTOGRAPH OF BREADBOARD CIRCUIT

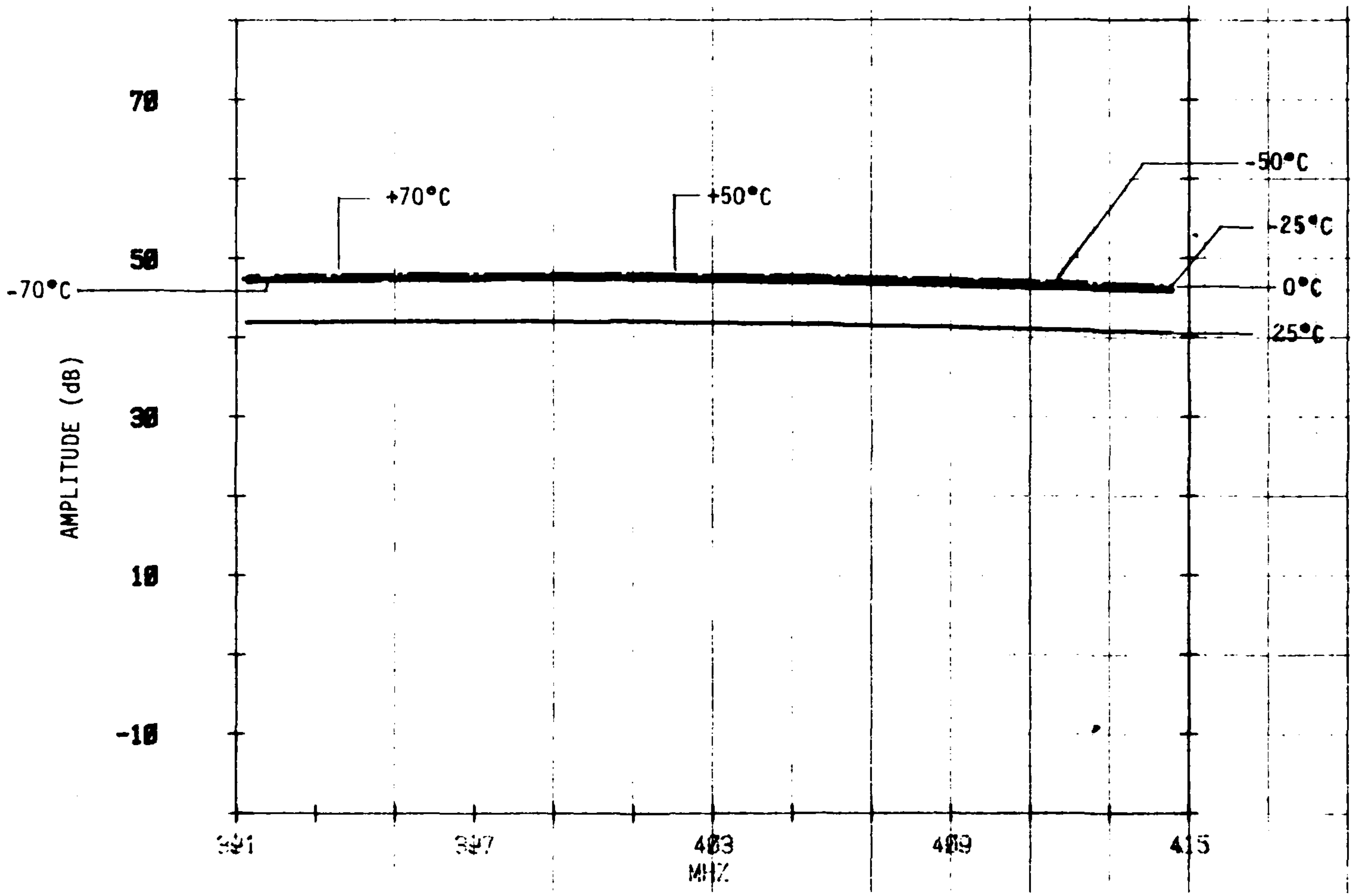


Figure 3-11. 403 MHz SAW AMP, V_{CC} = 12V, P_{IN} = -40 dBm

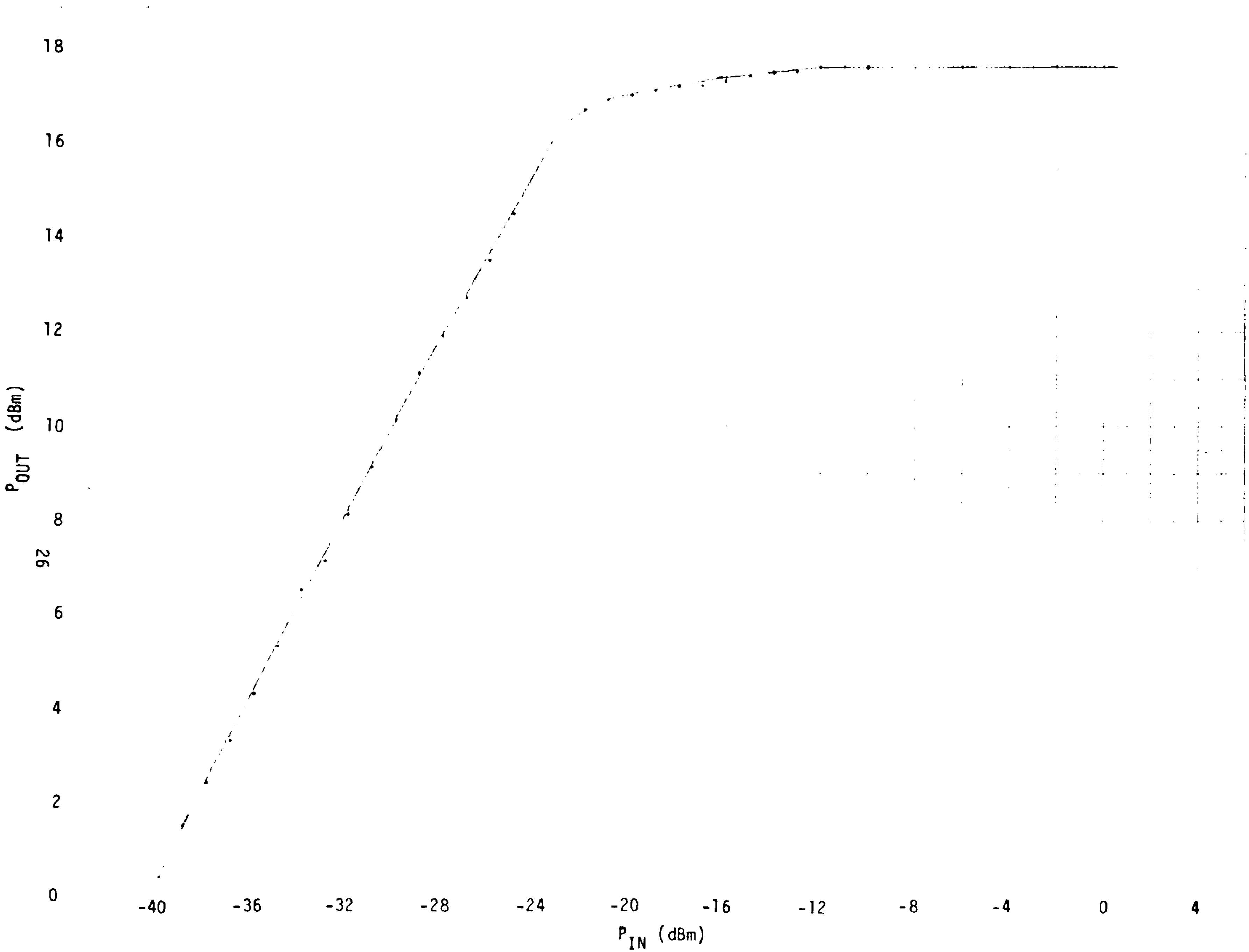


Figure 3-12. LOOP AMPLIFIER P_{OUT} vs P_{IN} (12V Bias)

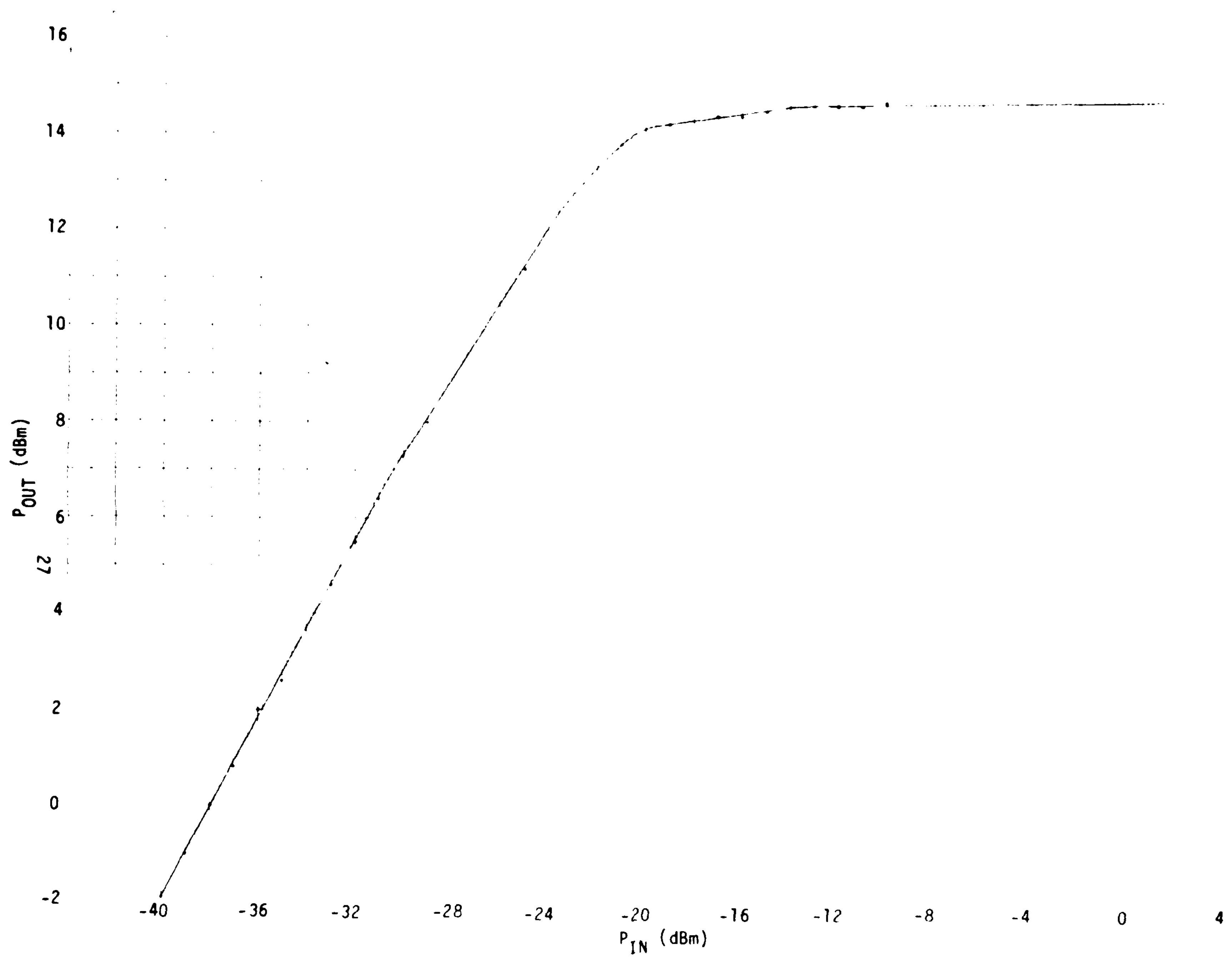


Figure 3-13. LOOP AMPLIFIER P_{OUT} vs P_{IN} (9V Bias)

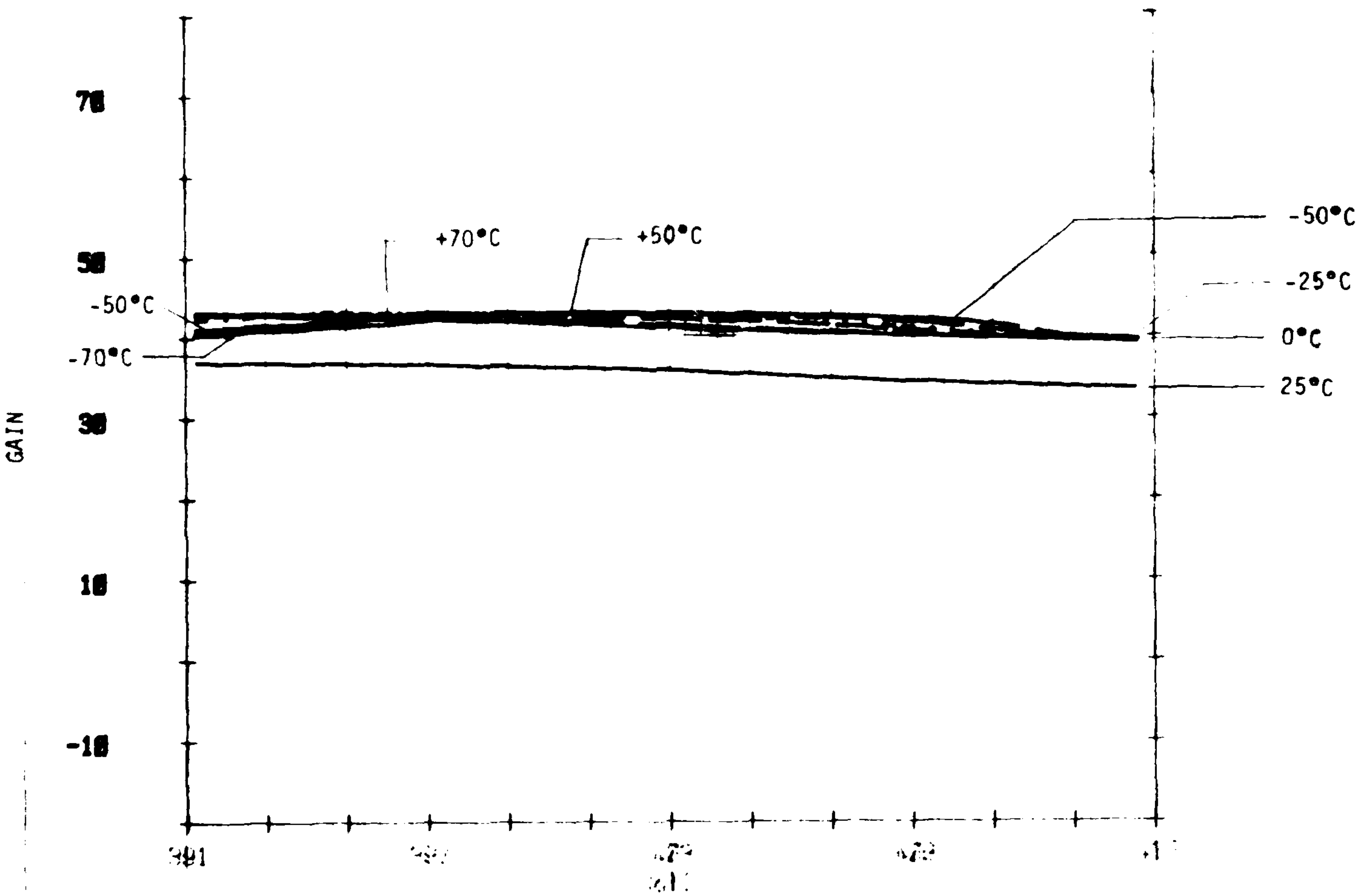


Figure 3-14. 403 MHz SAW AMP, V_{CC} = 12V, P_{IN} = -18 dBm

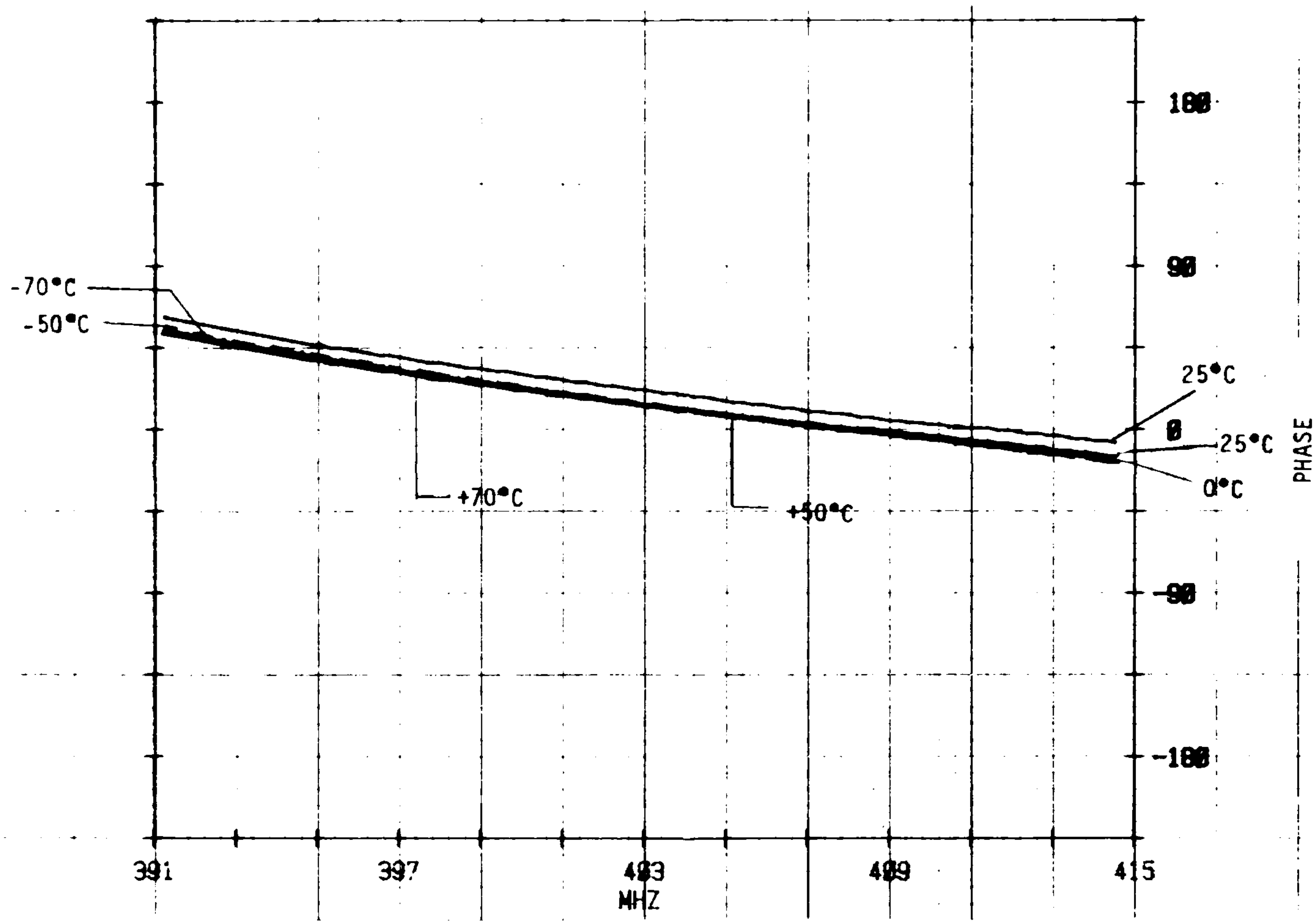


Figure 3-15. 403 MHz SAW AMP, V_{CC} = 12V, P_{IN} = -40 dBm

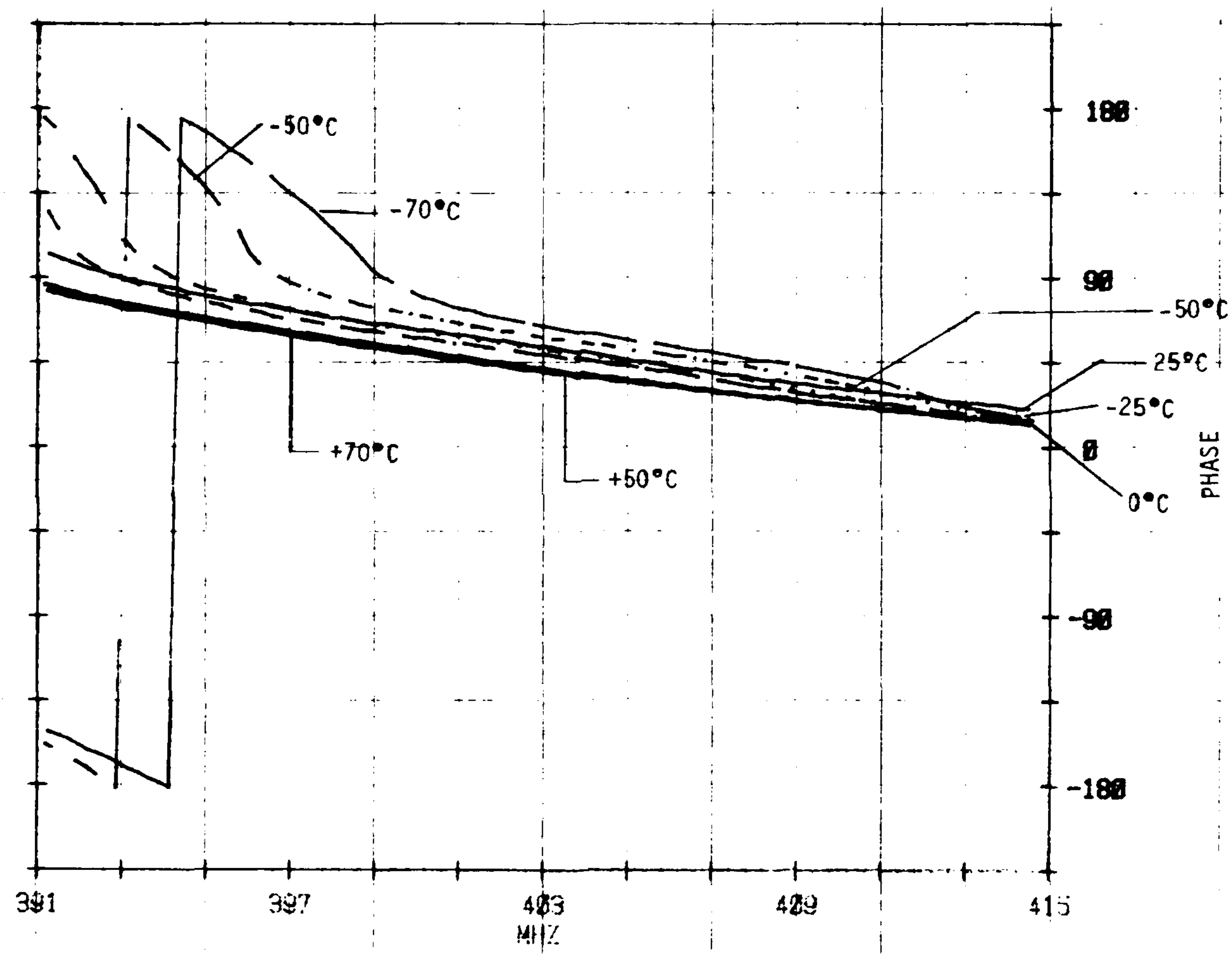


Figure 3-16. 403 MHz SAW AMP, V_{CC} = 12V, P_{IN} = -18 dBm

As the results show, the loop amplifier as designed is adequate for use in the SAW oscillator. A comparison of the measured and required performance is shown below:

Parameter	Required Performance	Measured Performance
Frequency Band	>350-450 MHz	>350-450 MHz
Gain	$\geq$40 dB	42-48 dB
P_{SAT}	+16.5 dBm	+14.5 dBm* (9V bias)
VSWR (In,Out)	$\leq$2.5:1	$\leq$2.0:1
V_{Supply}	12V	12V (regulated to 9V)

*The saturated output power with 12V bias is +17.5 dBm. The ILO has been designed to operate with lower injected power.

c. Phase Shifter

The phase shifter block diagram is shown in Figure 3-17.

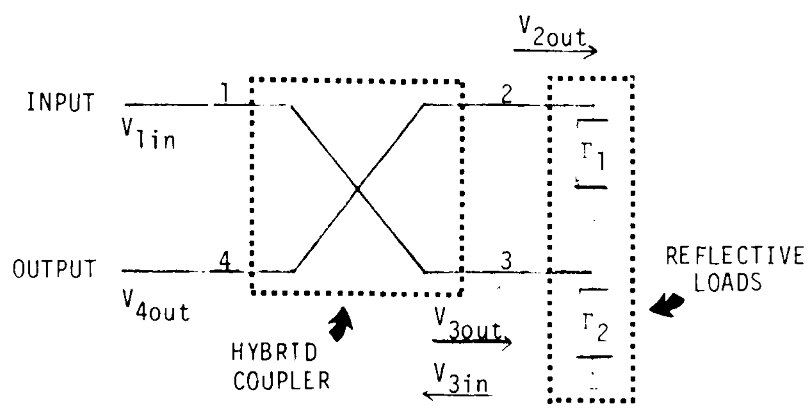


Figure 3-17. PHASE SHIFTER BLOCK DIAGRAM

The circuit consists of a hybrid coupler loaded with tunable, reflective loads. In this design, power incident at port 1 is split with equal amplitude, and 90° relative phase between ports 2 and 3. Since the loads at ports 2 and 3 are reflective, the power incident on these loads from ports 2 and 3 is reflected back into the coupler. The reflected signals experience a phase shift associated with the reflection coefficient of the loads, and since the loads are tunable this phase shift can be varied. The reflected signals entering the coupler at ports 2 and 3 add in phase at port 4 and add out of phase (cancel) at port 1. Therefore, this circuit will transfer a signal incident at port 1 to port 4 with a phase shift which is a function of the reflection coefficient of the loads.

To better understand the operation of this circuit, let $V_{1in} = Ae^{j\omega t}$ be the signal input to port 1. Then $V_{2out} = \frac{A}{\sqrt{2}} e^{j\omega t}$ and $V_{3out} = \frac{A}{\sqrt{2}} e^{j(\omega t + \pi/2)}$; i.e., half of the power input to port 1 goes to each of ports 2 and 3. If the networks connected to ports 2 and 3 have reflection coefficients of Γ_1 and Γ_2, respectively, then the signals input to ports 2 and 3 are given as

$$V_{2in} = \frac{A}{\sqrt{2}} e^{j\omega t} \Gamma_1 \qquad (3.1)$$

$$V_{3in} = \frac{A}{\sqrt{2}} e^{j(\omega t + \pi/2)} \Gamma_2 \qquad (3.2)$$

After traveling through the quadrature hybrid again, the signal levels out of ports 1 and 4 are given by

$$V_{1out} = \frac{A}{2} [e^{j\omega t} \Gamma_1 + e^{j(\omega t + \pi)} \Gamma_2] \qquad (3.3)$$

$$V_{4out} = \frac{A}{2} [e^{j(\omega t + \pi/2)} \Gamma_1 + e^{j(\omega t + \pi/2)} \Gamma_2]. \qquad (3.4)$$

It is now apparent that if $\Gamma_1 = \Gamma_2$, V_{1out} equals zero and all power incident at port 1 appears at port 4. More importantly, notice that V_{4out} is a function of the load reflection coefficients. The relative phase of the output signal is therefore determined by the phase of the load reflection coefficient.

In practice the loads are made identical but some small difference in reflection coefficient will exist. The loads also will be lossy. Consider the case where loads are neither equal nor ideal. Let

$$\Gamma_1 = \rho e^{j\theta_1} \tag{3.5}$$

$$\Gamma_2 = \rho e^{j\theta_2} \tag{3.6}$$

For this case

$$V_{4out} = \frac{A\rho}{2}\left[e^{j(\omega t + \pi/2)}\left(e^{j\theta_1} + e^{j\theta_2}\right)\right] \tag{3.7}$$

or

$$V_{4out} = A\rho \cos\frac{\theta_1 - \theta_2}{2}\, e^{j\left(\omega t + \pi/2 + \frac{\theta_1 + \theta_2}{2}\right)} \tag{3.8}$$

The phase shift from port 1 to port 4 is therefore $\frac{\pi}{2} + \frac{\theta_1 - \theta_2}{2}$. The loss through the phase shifter is $20 \log \left(\rho \cos\frac{\theta_1 - \theta_2}{2}\right)$ dB. For small differences in the angles of the reflection coefficients, θ_1 and θ_2, the loss will be determined by ρ. For a 90° difference in θ_1 and θ_2, 3 dB of additional loss will occur.

The design of the hybrid coupler itself can be either distributed or lumped. For this application a lumped element design was chosen to minimize size. A schematic of this coupler is shown in Figure 3-18

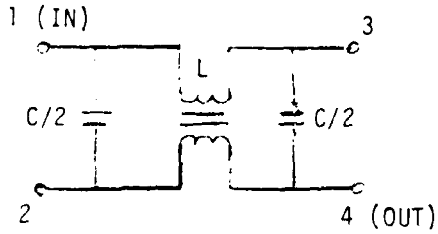


Figure 3-18 COUPLER SCHEMATIC

For this design

$$Z_o = \sqrt{\frac{L}{C}} \tag{3-9}$$

and

$$\omega_o = \sqrt{\frac{1}{\sqrt{LC}}} \tag{3-10}$$

where

Z_o = characteristic impedance

ω_o = radian frequency at center band.

For the phase shifter, $\omega_o = 2\pi(403 \times 10^6)$, and $Z_o = 50\Omega$. Therefore

$$Z_o = \sqrt{\frac{L}{C}} = 50 \tag{3-11}$$

$$\omega_o = \frac{1}{\sqrt{LC}} = 2\pi(403 \times 10^6) \tag{3-12}$$

and

$$\begin{aligned} L &= 19.7 \text{ nH} \\ C &= 7.9 \text{ pF} \end{aligned} \tag{3-13}$$

This coupler has been built and tested. Tests indicate that using 10 pF capacitors will produce an equal -3.7 dB power split with relative phase of 88°. Using 8.2 pF capacitors produces a 90° relative phase split but the amplitude split is unbalanced by 0.4 dB to -3.6 dB and -4.0 dB. Measured results for a breadboard coupler are shown in Figure 3-19.

The design of the circuit which will load the hybrid coupler is shown in Figure 3-20. This load consists of a shunt indictance, a varactor, and a DC blocking capacitor. The reflection coefficient of the load is

$$\rho = \frac{Z_L - Z_o}{Z_L + Z_o} \tag{3.14}$$

where

Z_L = load impedance $\left(\frac{Z_{ind} Z_{cap}}{Z_{ing} + Z_{cap}}\right)$

Z_o = system characteristic impedance (50 ohms typical)

The choice of inductor and varactor will determine the maximum phase variation of the phase shifter and tuning range of the oscillator For maximum phase variation, the inductor-varactor combination is designed to resonate in the center of the varactor's tuning range. However, such a design results in a nonlinear phase-voltage relationship due to the nonlinear capacitance-voltage relationship of the varactor. To simplify temperature compensation and to insure more linear frequency modulation, it is desirab' to design a load with a near linear phase voltage relationship. By increasing the inductance value such that LC resonance occurs at the lower extreme of the capacitance range, a more linear relationship is achieved. Such a design has been investigated for this application but total phase shift was found to be inadequate.

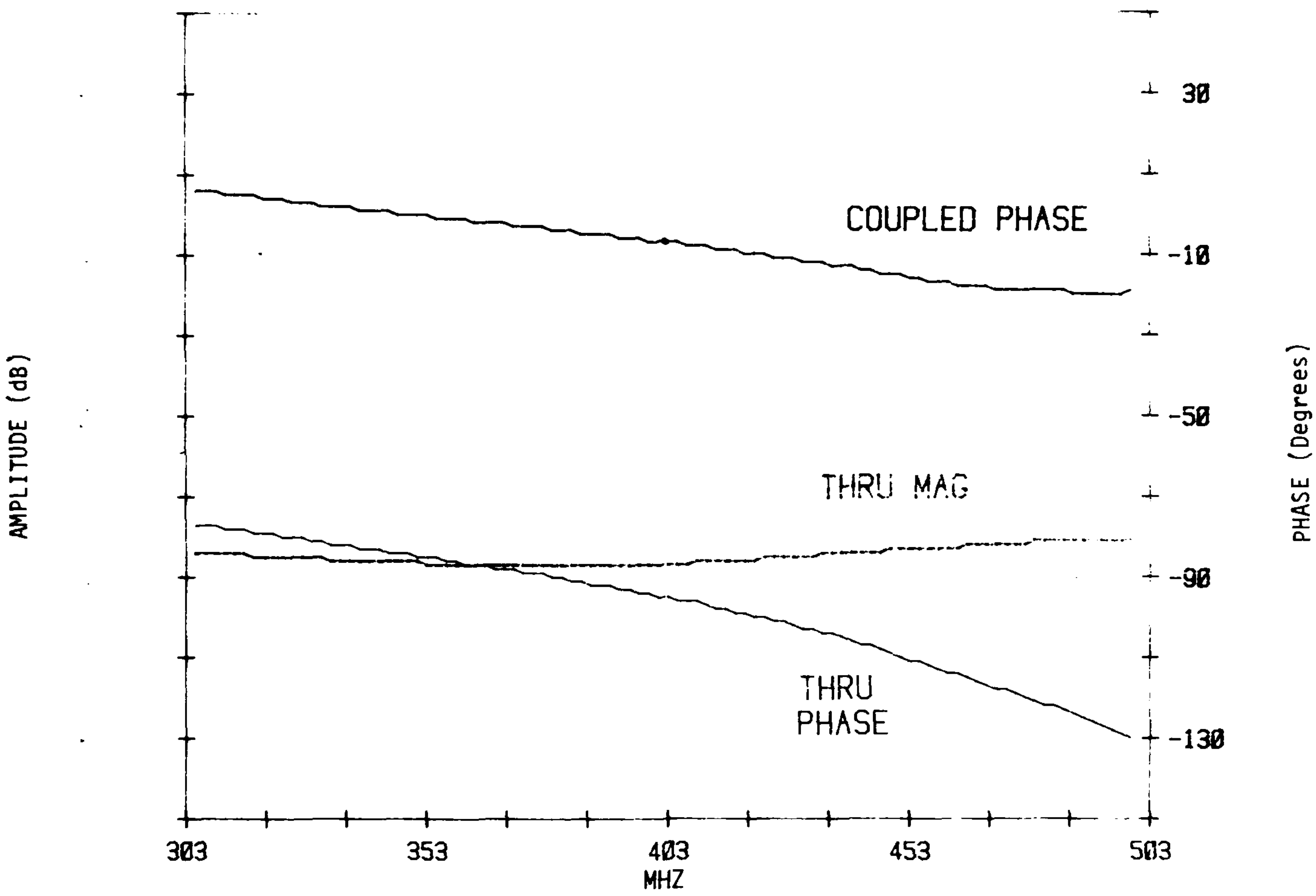


Figure 3-19. 403 MHz TWISTED WIRE COUPLER

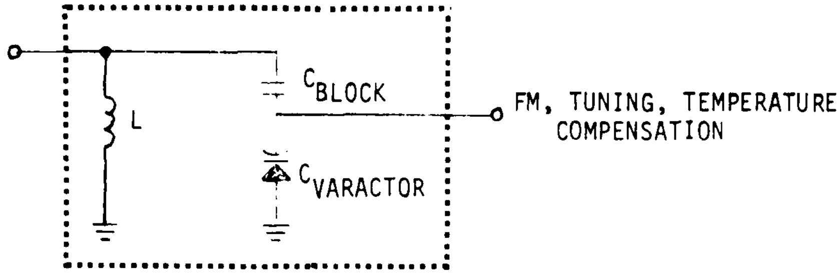


Figure 3-20. COUPLER LOAD

To select the LC combination most suitable the varactor diodes were first characterized. Reflection coefficient as a function of voltage is shown in Figure 3-21. Note that using the varactor alone would produce only a 60° phase shift for a 0-10V tuning range. This characterization also indicates the diodes have approximately 0.5 ohm series resistance which will contribute to the overall phase shifter loss. To resonate this capacitance an inductor of approximately 8 nH was used. Assuming 0.02 ohm series resistance in the inductor, a computer model of this load predicted the performance shown in Figure 3-22. This compares well with the measured results shown in Figure 3-23

The total phase shifter, consisting of the coupler and the loads discussed above, has been constructed and tested. A photograph of the breadboard phase shifter is shown in Figure 3-24 Test results for two such phase shifters cascaded are shown in Figure 3-25. This figure is a plot of both loss and phase through the circuit as a function of tuning voltage. The data shows loss varying from approximately 5 dB at 0.5V down to 2 dB at 10V. The decreasing loss results from a decrease in diode series resistance with increasing reverse bias. The data also shows phase varying from 18° at 0.5V to ±180° at just below 2V, to -36° at 5V and back to +18° at 10V. A full 360° shift has been realized with this cascade of two phase shifters.

One of the difficulties encountered when using varactor diodes is their capacitance variation with temperature. This variation translates into a change in reflection coefficient and therefore a change in phase through the circuit.

NAME	TITLE	DWG. NO
SMITH CHART FORM 82-BSPR (9-66)	KAY ELECTRIC COMPANY PINE BROOK N.J. ©1966 PRINTED IN U.S.A.	DATE

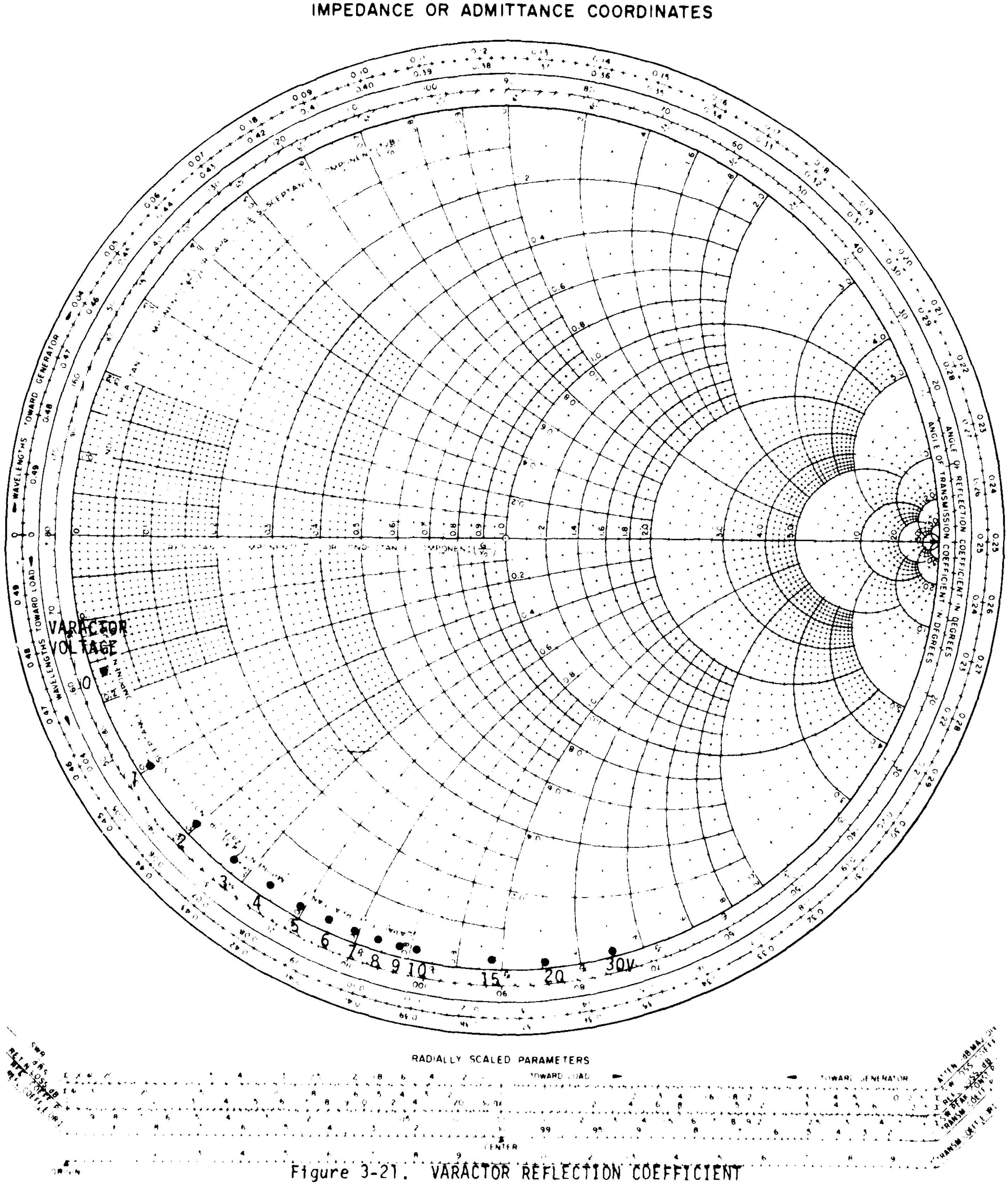


Figure 3-21. VARACTOR REFLECTION COEFFICIENT

Figure 3-22.

COMPUTER-PREDICTED LOAD REFLECTION COEFFICIENTS

C (@V)	Magnitude	Angle	Loss
5.0	.995	122.8	-.05
10.0 (@ 6V)	.981	100.5	-.17
15.0 (@ 3V)	.936	59.4	-.57
20.0 (@ 2V)	.867	-7.2	-1.24
25.0 (@ 1V)	.865	-69.9	-1.26
30.0	.896	-106.3	-.95
35.0	.920	-126.2	-.73
40.0	.934	-138.0	-.59
45.0	.944	-145.7	-.50
50.0 (@ 0V)	.950	-151.1	-.44

NAME	TITLE	DWG. NO
SMITH CHART FORM 82-BSPR(9-66)	KAY ELECTRIC COMPANY, PINE BROOK, N.J. © 1966 PRINTED IN U.S.A.	DATE

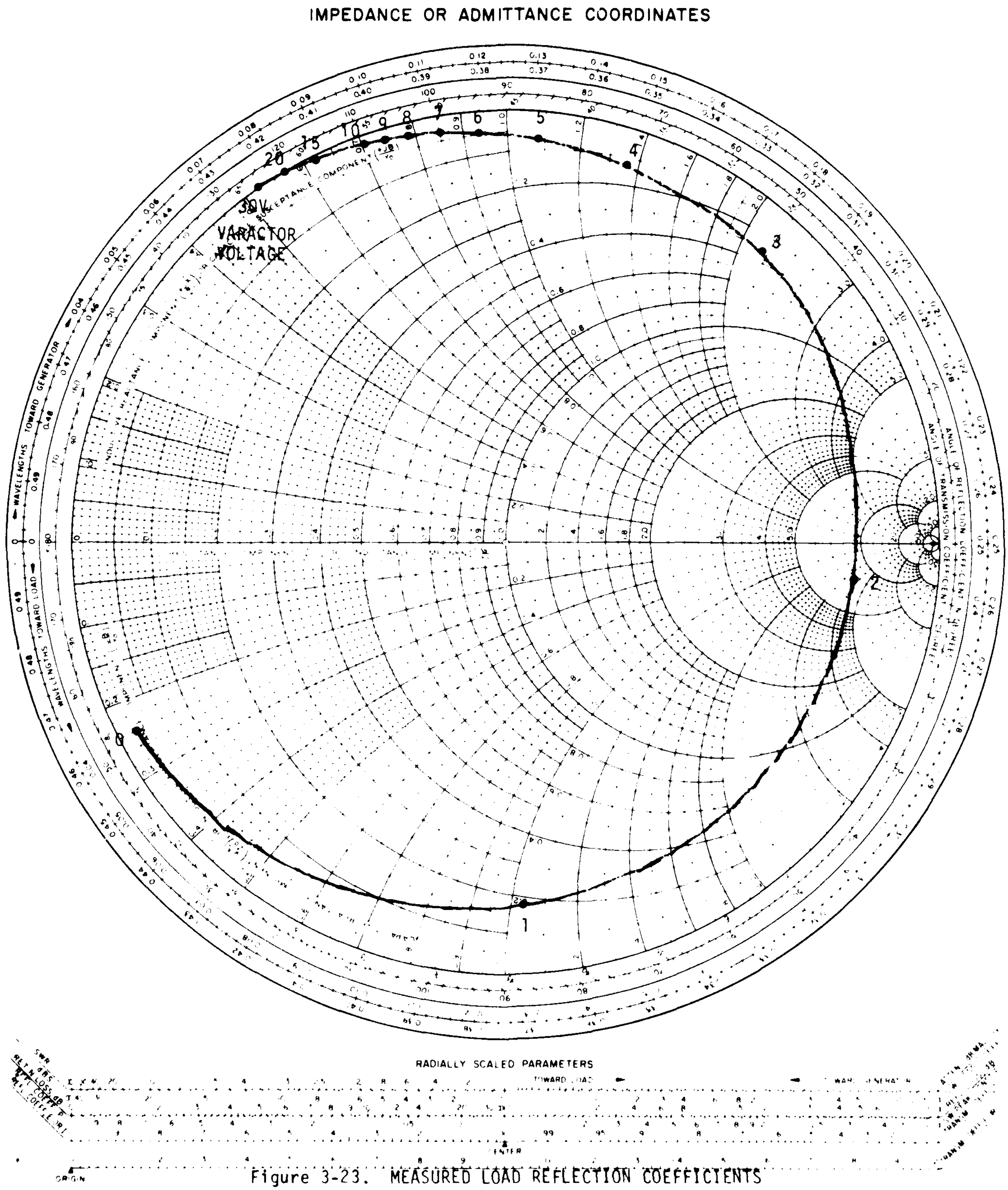


Figure 3-23. MEASURED LOAD REFLECTION COEFFICIENTS

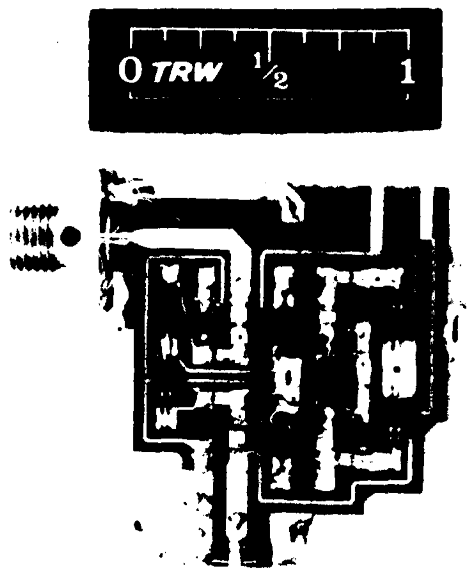


Figure 3-24. PHOTOGRAPH OF BREADBOARD PHASE SHIFTER

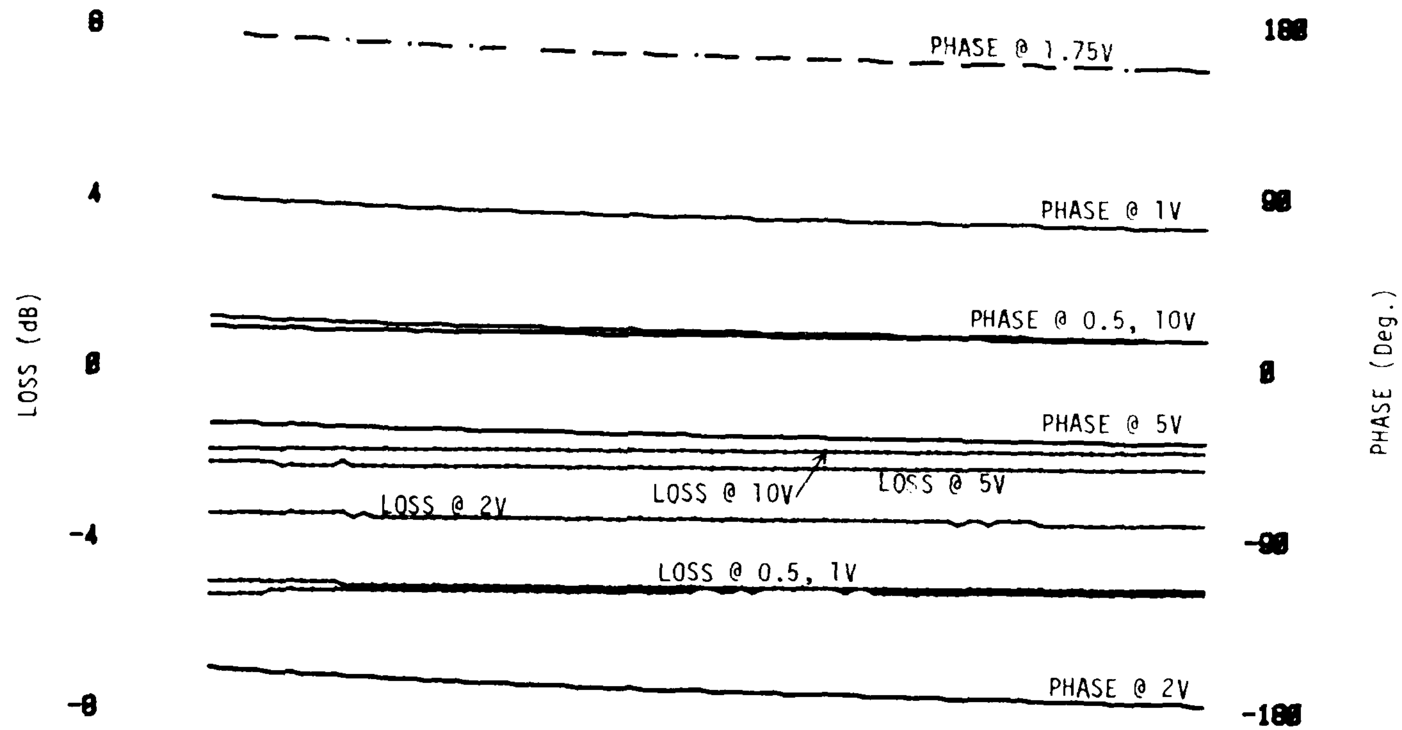


Figure 3-25. 403 MHz BREADBOARD DOUBLE PHASE SHIFTER

The frequency of the oscillator therefore will drift with temperature. Tests have been run on the [illegible] phase shifter to characterize temperature performance. The detailed results are included in the Appendix for reference and are summarized with the graph in Figure 3-26. It is the frequency drift with temperature caused by varactor change which requires that a temperature compensating network be used. The compensating voltage will be summed with the tuning and modulation voltages and applied to the varactor. As mentioned earlier the DC circuitry including the temperature compensation network has not yet been designed.

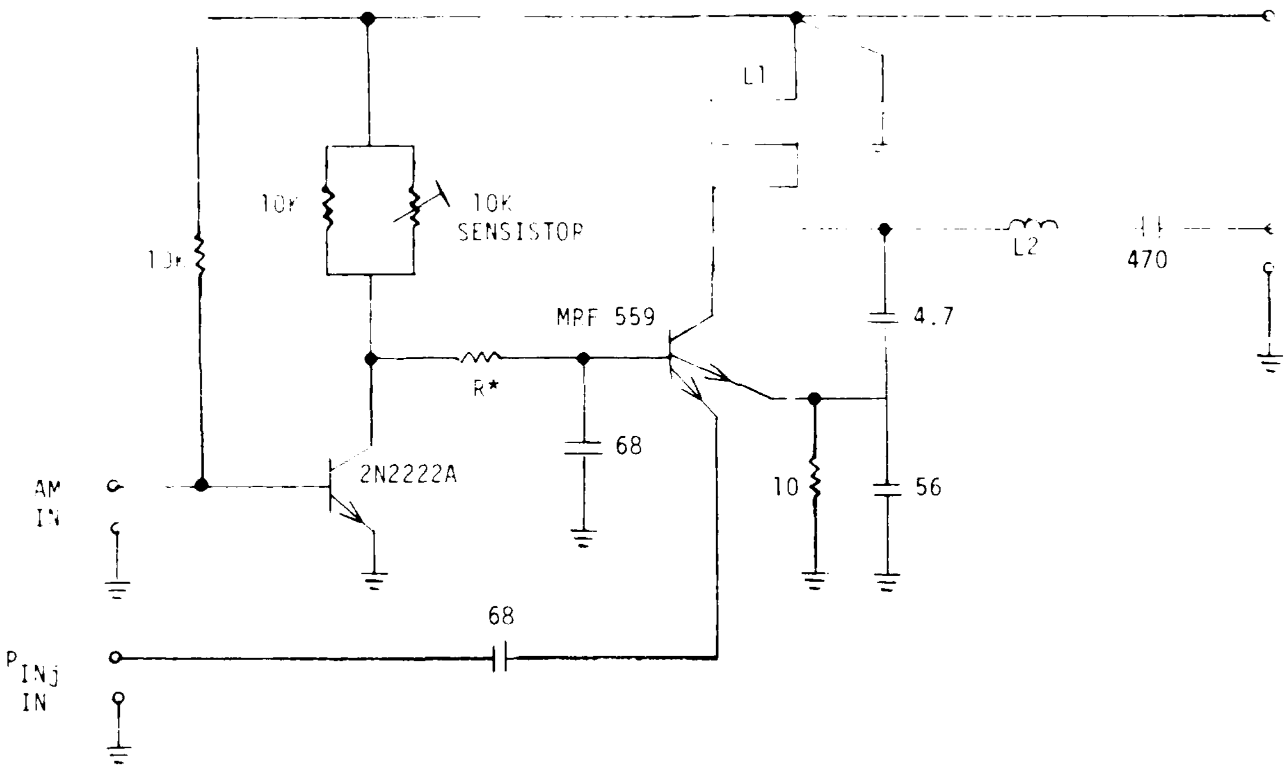
As the results in this section indicate, the design of the phase shifter is complete and performance is adequate for the SAW oscillator application. A comparison of measured and required performance is shown below.

Parameter	Requirement	Performance
Frequency	[illegible] MHz	[illegible] MHz
Phase Shift	360	[illegible]
Loss	6 dB	[illegible] to 5 dB
Tuning Voltage	1-10V	[illegible]

d. Injection Locked Oscillator

The injection locked oscillator (ILO) is used to amplify the output of the SAW oscillator to the required 200 mW (+23 dBm). Pulse amplitude modulation is also accomplished in the ILO. A schematic of the circuit is shown in Figure 3-27

The oscillator is of the form of a Colpitts with a resonant tank in the collector circuit and feedback to the emitter. The injection locking signal is applied to the emitter-base junction.



L2 = 10 turns #30 wire on #72 drill (25 mils diameter)

R* = SIT resistor for bias (~100 mA), 1K-5K ohms.

L1 = printed inductor.

Figure 3-27. 403 MHz ILO

This circuit has been designed, built and tested. A photograph of the breadboard circuit is shown in Figure 3-28. Test results are shown in Figures 3-29 through 3-31 Figure 3-29 is a plot if injection locking bandwidth vs injection locking power. Figure 3-30 shows injection locking bandwidth vs temperature. Output power vs frequency is shown in Figure 3-31.

Pulse amplitude modulation characteristics are shown in Figures 3-32 and 3-33. Time waveforms are shown in Figures 3-32a through 3-32e, while frequency spectrum is shown in Figures 3-33a through 3-33d.

As the data shows, the ILO is adequate for this application. A comparison of measured and required performance is shown below:

Parameter	Requirement	Performance
Center Frequency	403 MHz	403 MHz (adjustable)
Power Out	23 dBm	>+24 dBm
Injection Locking Bandwidth	16 MHz	49 MHz (@ 25°C, +12 dBm)
P_{inj}	+13 dBm	+12 dBm
V_{supply}	+12V	+12V

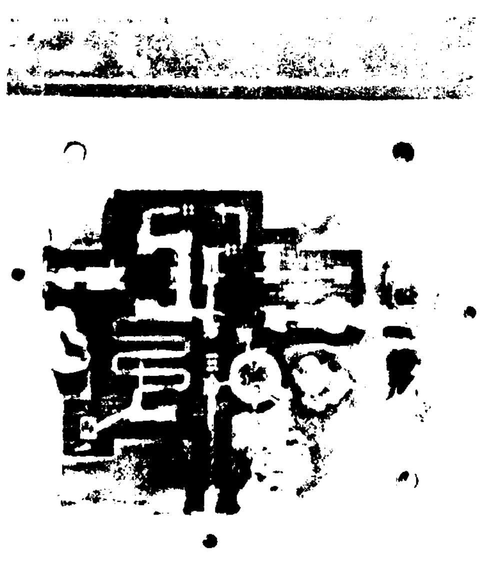


Figure 3-28. PHOTOGRAPH OF ILO BREADBOARD CICUIT

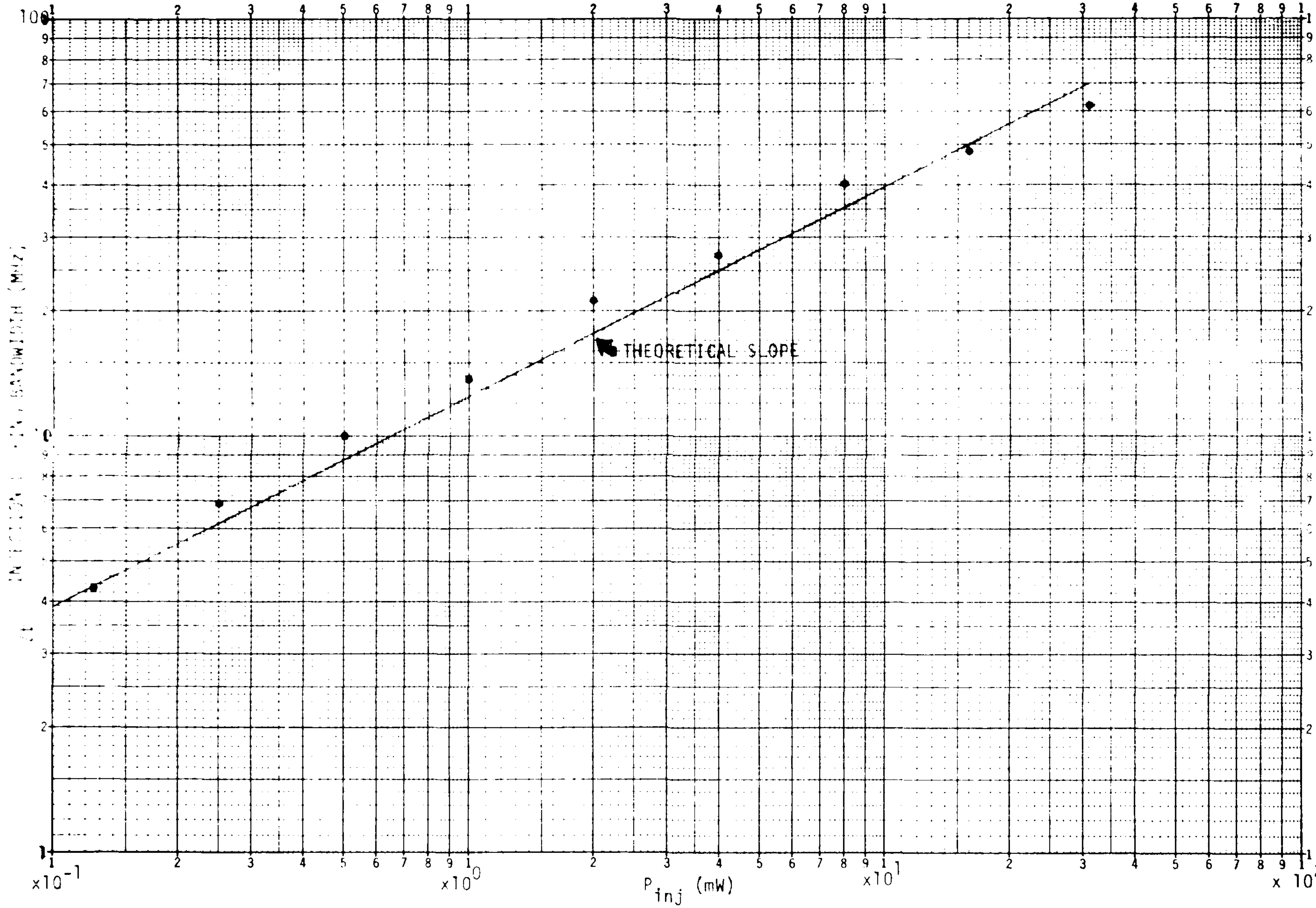


Figure 3-29. INJECTION LOCKING BANDWIDTH vs INJECTION POWER

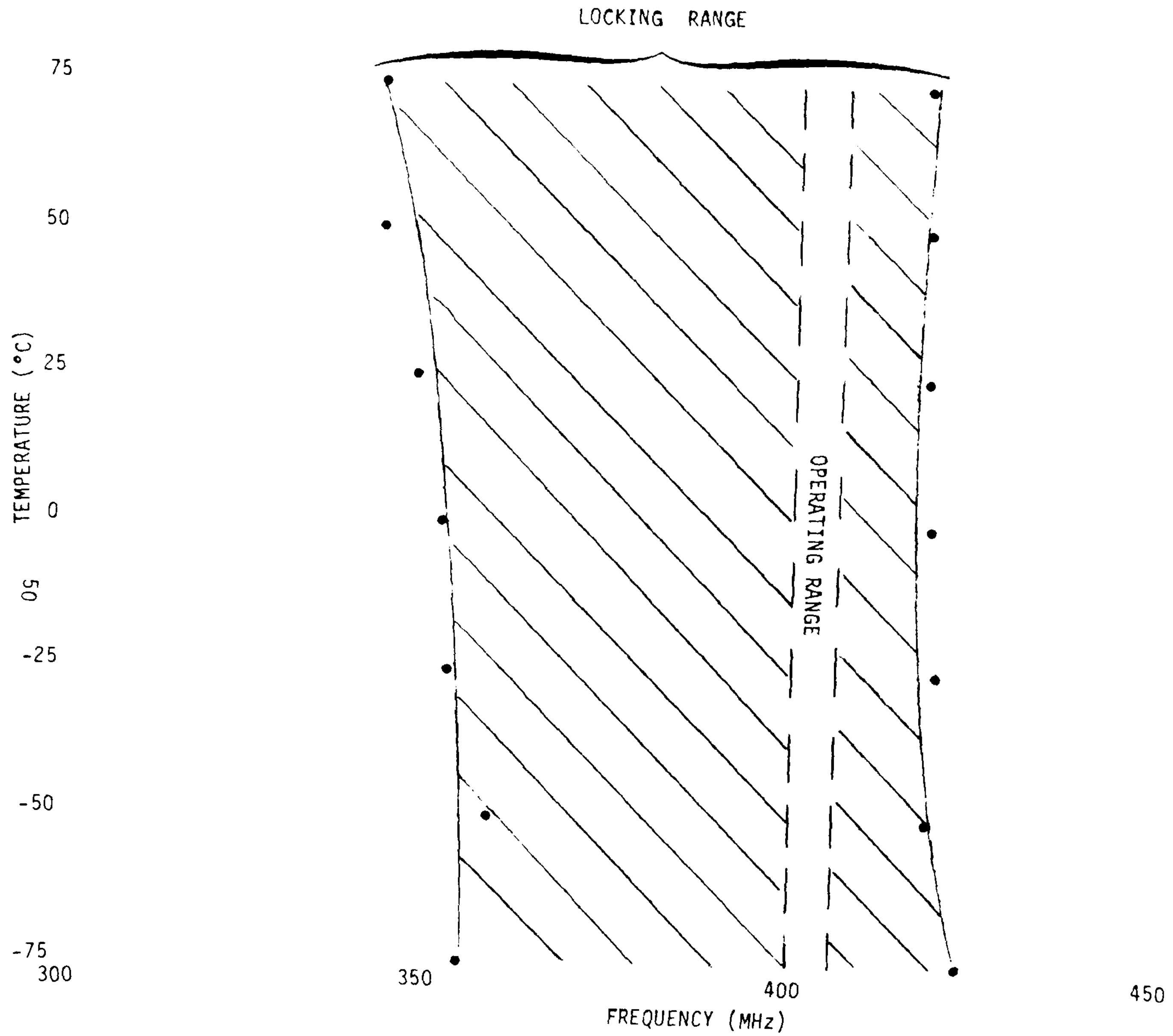


Figure 3-30. INJECTION LOCKING BANDWIDTH vs TEMPERATURE

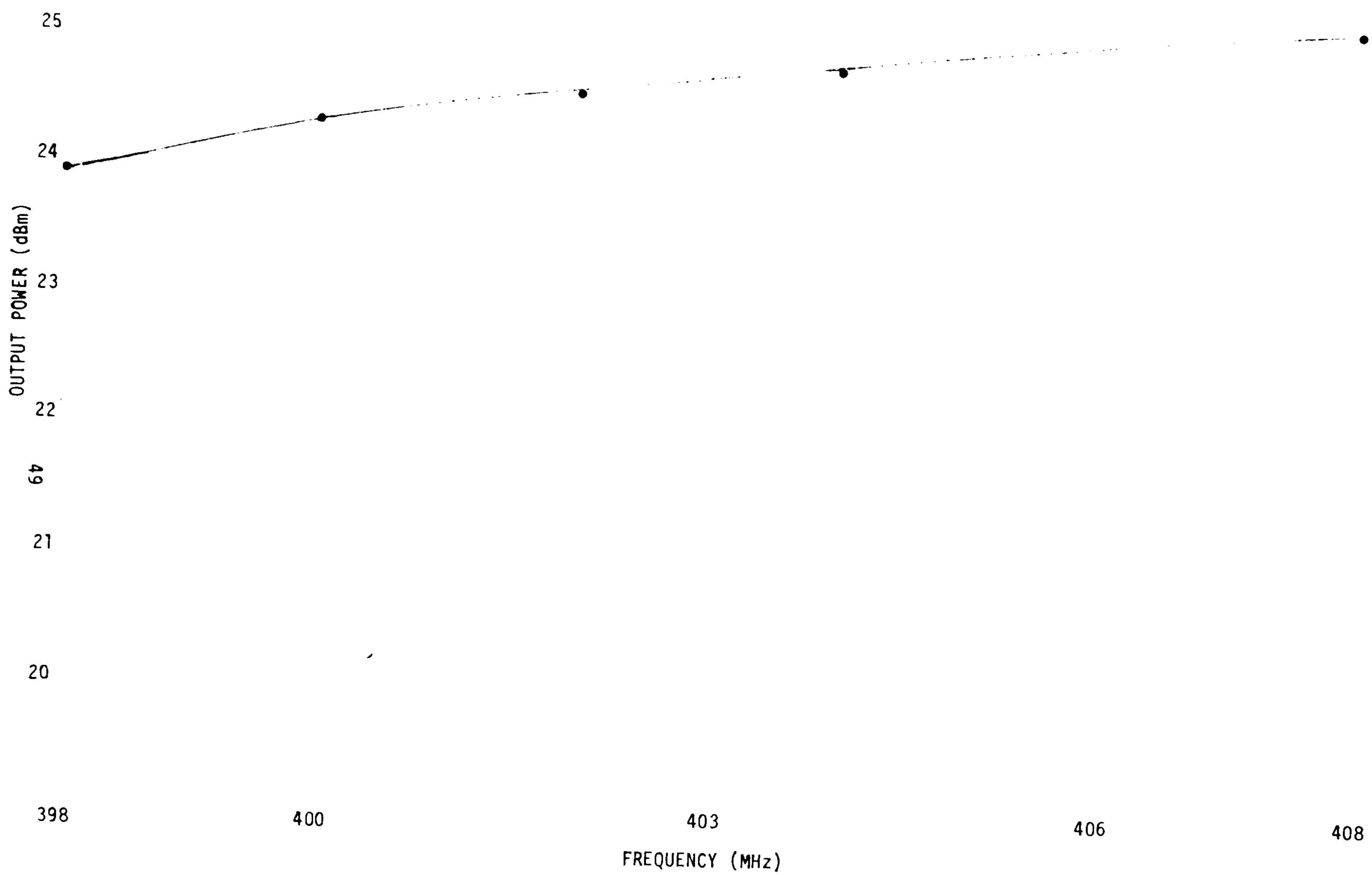
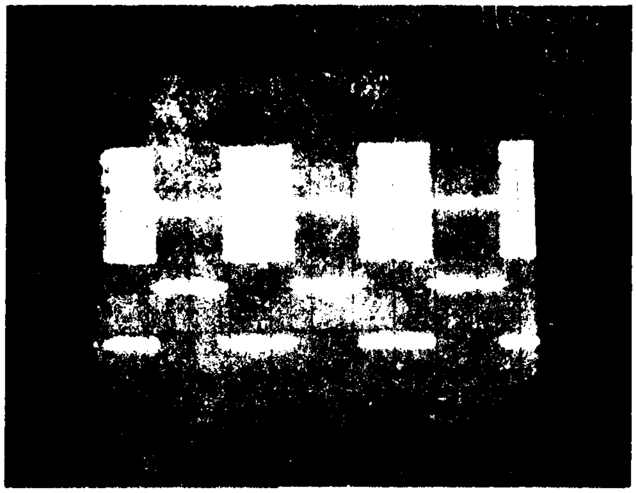
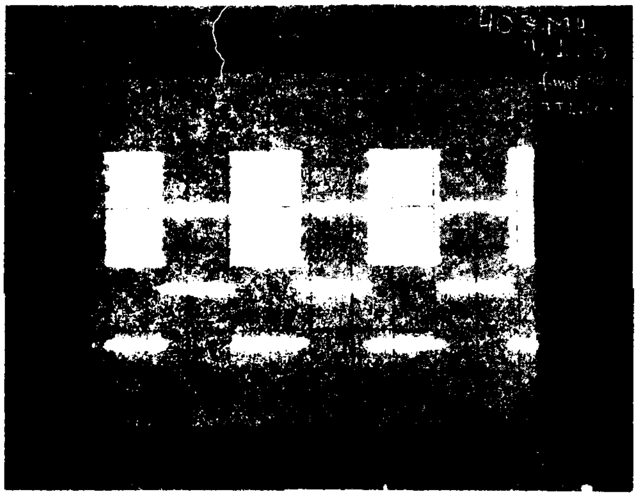


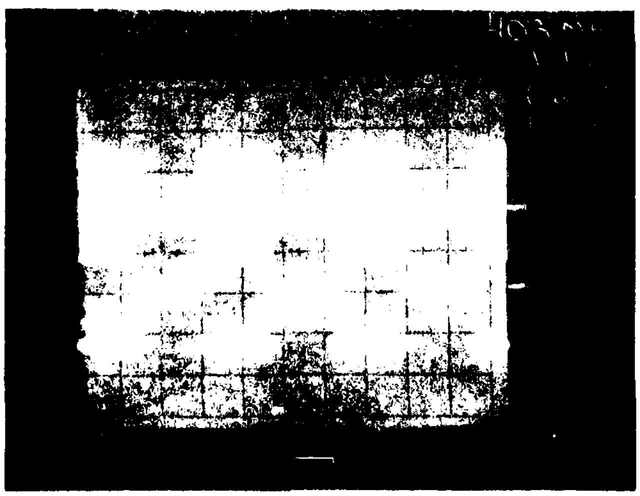
Figure 3-31. OUTPUT POWER vs FREQUENCY



(a) Modulation Frequency = 30 Hz

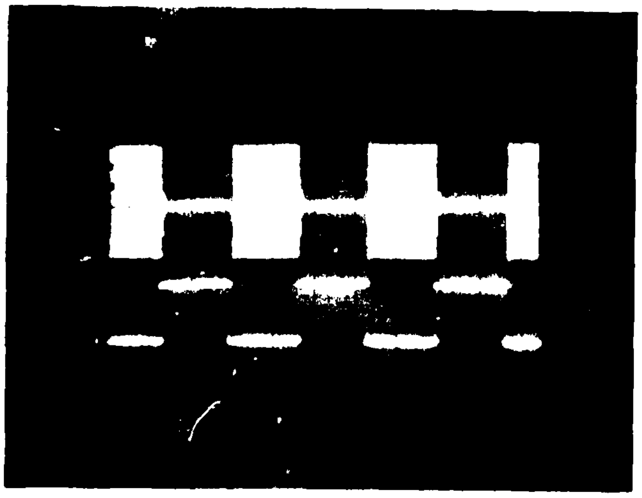


(b) Modulation Frequency = 300 Hz

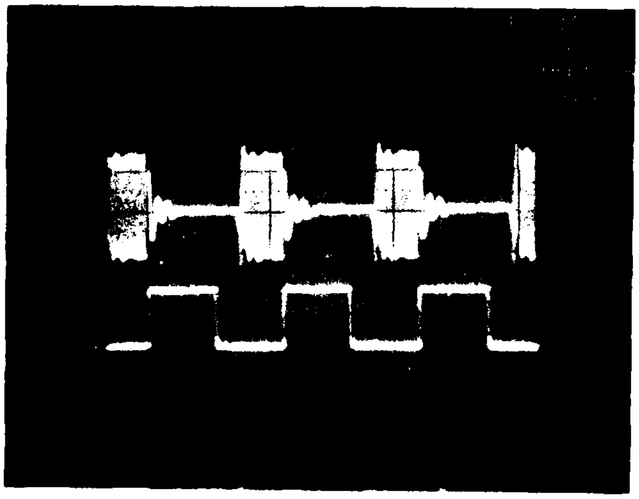


(c) Modulation Frequency = 3 kHz

Figure 3-3[illegible]. [illegible] AMPLITUDE MODULATION TIME WAVEFORMS

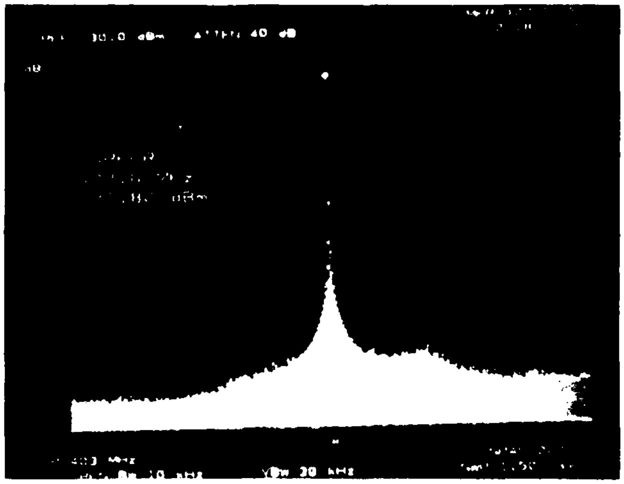


(d) Modulation Frequency = 30 KHz



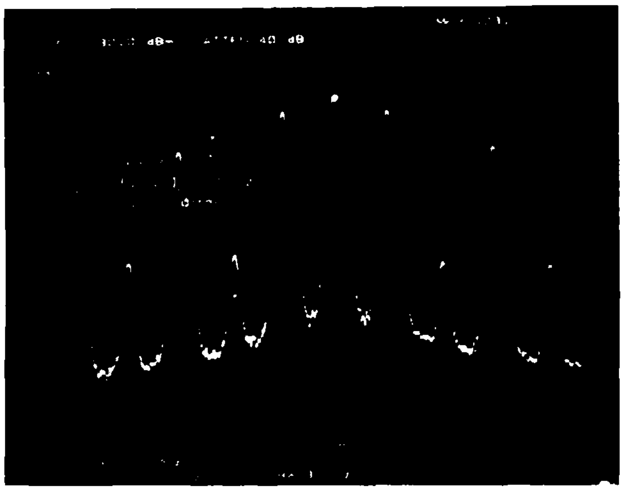
(e) Modulation Frequency = 300 KHz

Figure 3-32. ILO AMPLITUDE MODULATION TIME WAVEFORMS (Continued)



(a) 200 MHz Sweep Width

(b) 1 MHz Sweep Width



(c) 100 KHz Sweep Width

Figure 3-33. ILO AMPLITUDE MODULATION FREQUENCY SPECTRUM
(MODULATION FREQUENCY = 10 KHz)

4.0 CONCLUSION

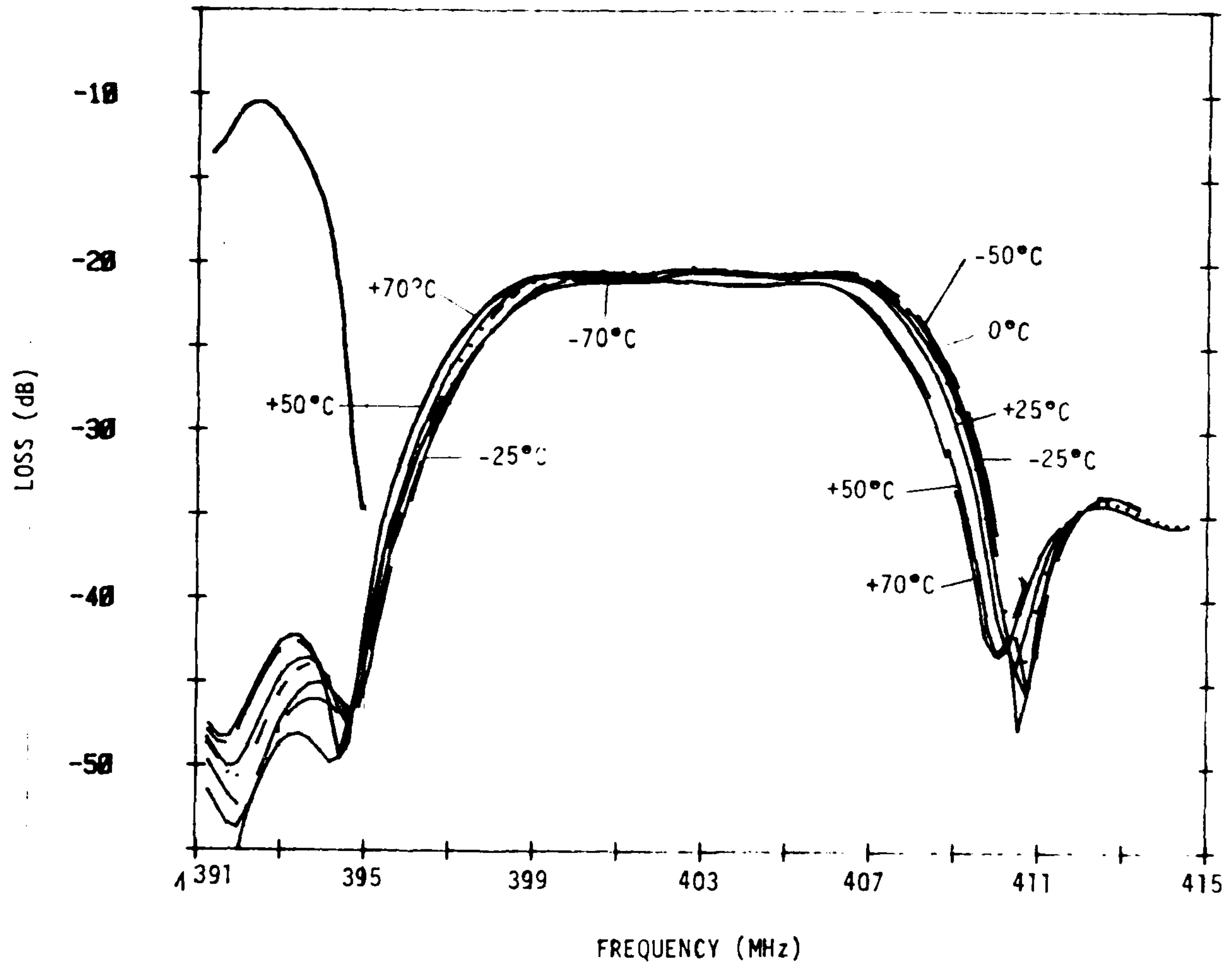
The RF circuitry described in this report has been adequately developed to be used in the construction of the 403 MHz SAW Oscillator. A number of difficulties which were encountered during the circuit development should be noted. The initial loop design did not adequately take into account the delay in loop components other than the SAW. The margin in mode spacing was therefore inadequate to assure a single oscillator output frequency. Both the SAW matching circuit and the loop amplifier contributed significantly to this additional delay. The sensitivity of the loop amplifier phase to bias - in the saturated operating condition - was also not anticipated. Regulation of the amplifier bias was added after this phenomenon was observed (see Appendix B). The phase shifter construction was not trivial. Performance of the circuit is dependent on both the inductance and coupling of the coil wires. Turns per inch and twists per inch are both critical. Once these parameters are determined, construction and performance of the coupler are very repeatable.

One observation regarding the temperature stability of the oscillator circuitry should be made. The requirement for FM has made achieving the required stability challenging. Frequency modulation requires electronic tuning in the oscillator loop. The varactors used for this tuning are the most unstable components in the oscillator. It is primarily their capacitance variation with temperature which requires a temperature compensation network to be used. Were the radiosonde system to require AM only, a mechanical phase shifter could be used for tuning and the stability of the oscillator would primarily reflect the SAW delay line temperature variation and not that of the phase shifter. Designing a mechanical phase shifter is far easier than compensation for the varactors.

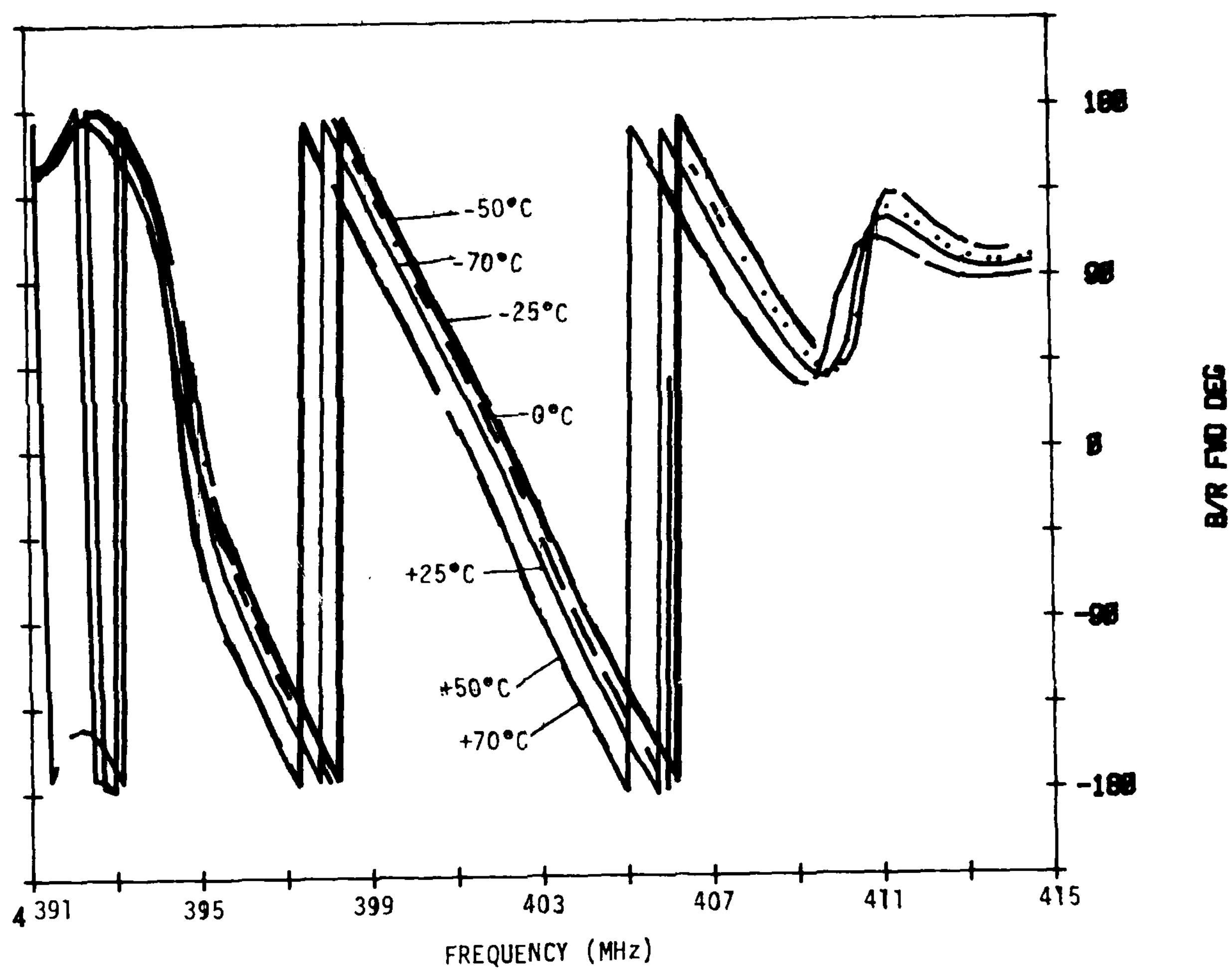
APPENDIX A

SAW PERFORMANCE vs TEMPERATURE MEASUREMENTS

MATCHED SAW PASSBAND VARIATION WITH TEMPERATURE



MATCHED SAW PHASE vs TEMPERATURE

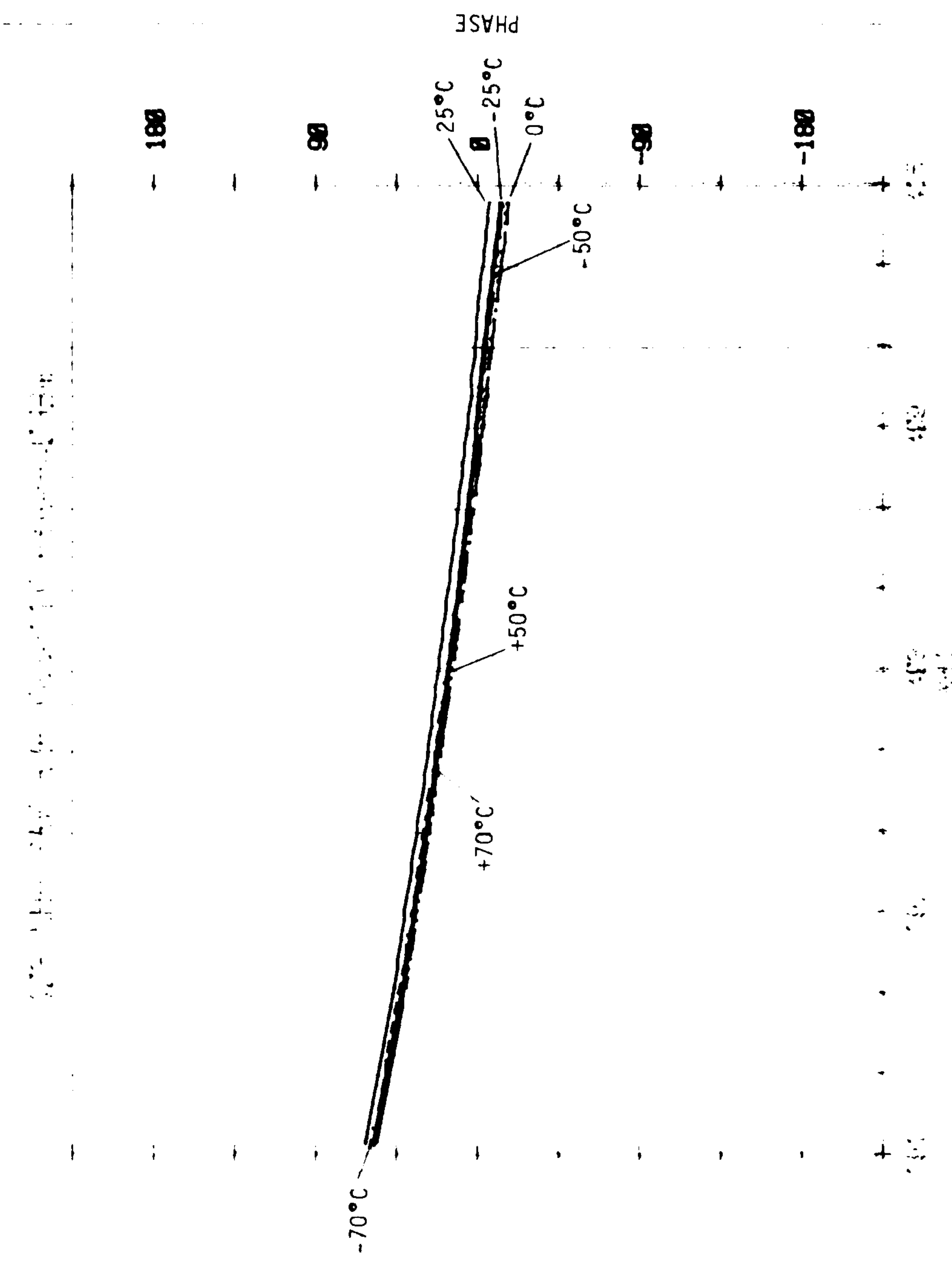


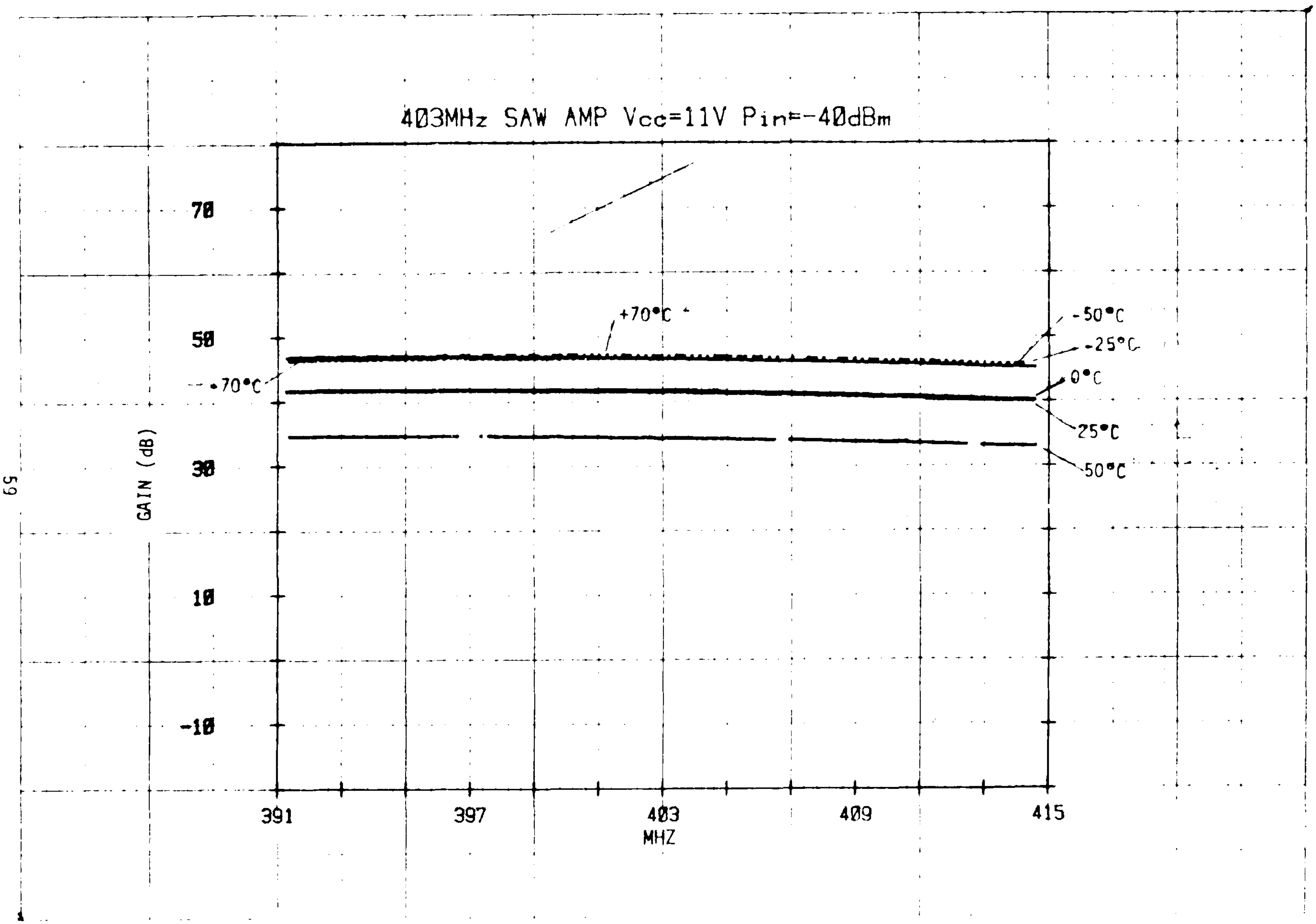
APPENDIX B

AMPLIFIER PERFORMANCE

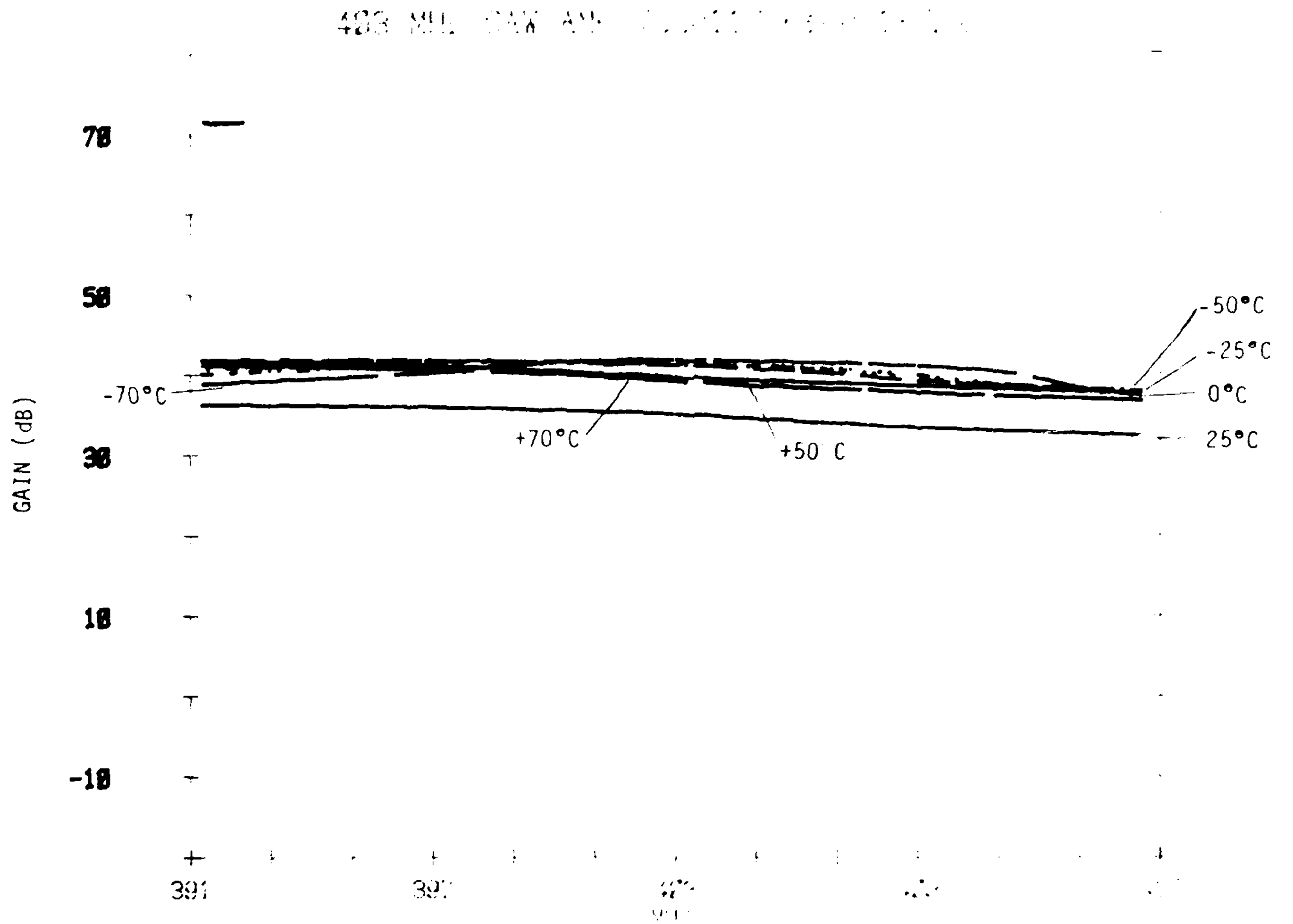
vs

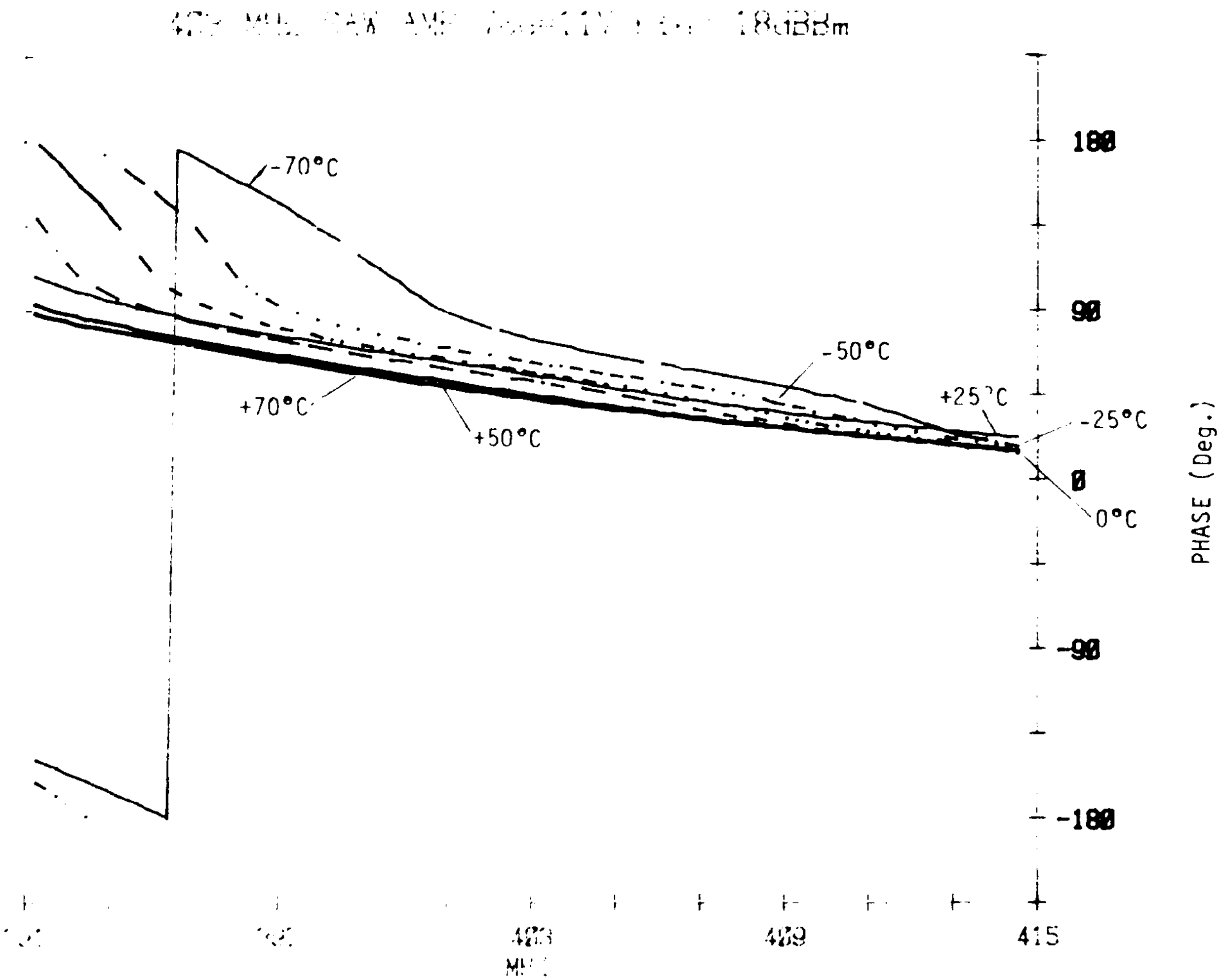
SUPPLY VOLTAGE AND TEMPERATURE

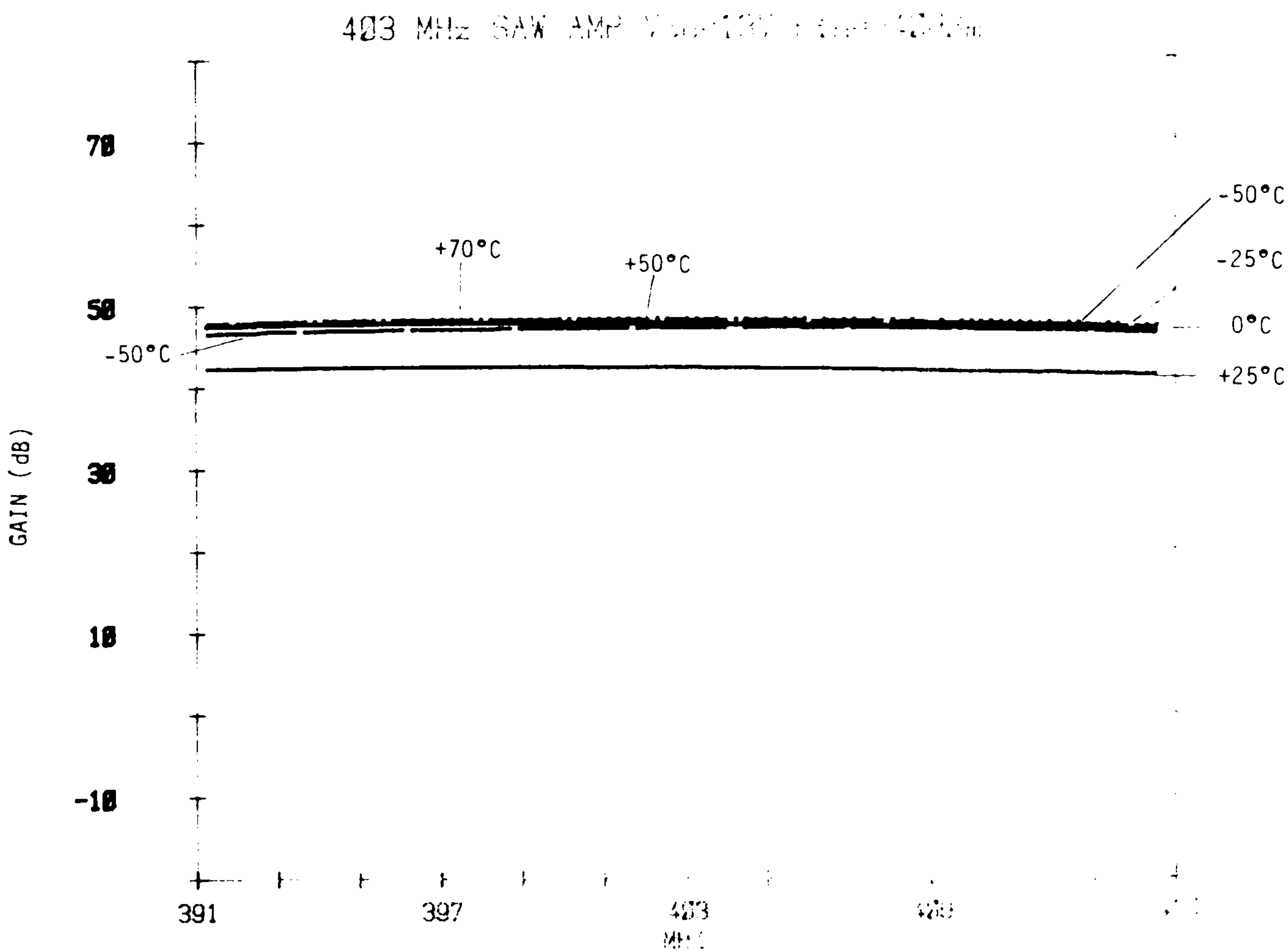

PHASE
180
90
0
-90
-180
25°C
-25°C
0°C
-50°C
+50°C
+70°C
-70°C

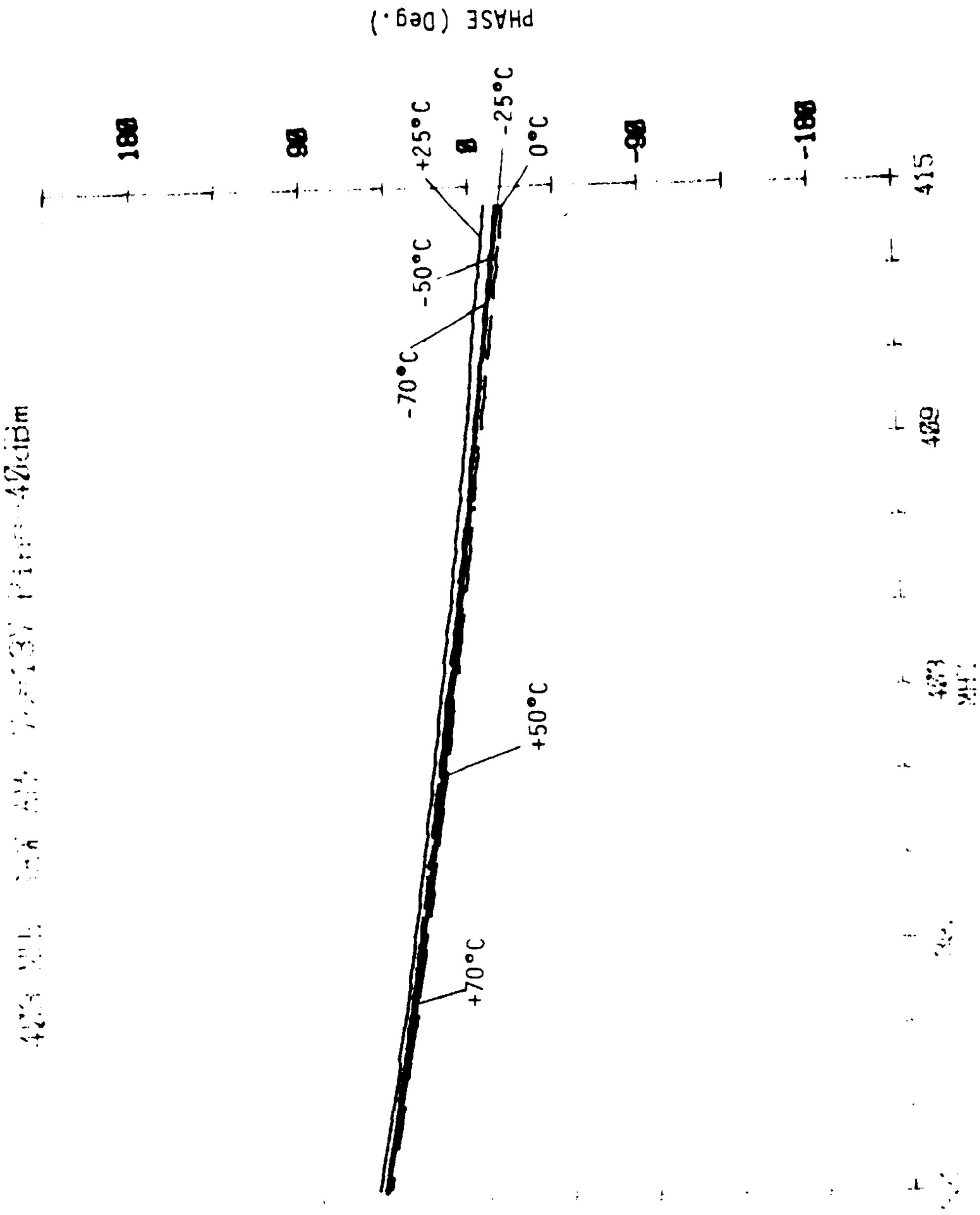


403MHz SAW AMP Vcc=11V Pin=-40dBm
70
50
30
10
-10
GAIN (dB)
+70°C
-50°C
-25°C
0°C
25°C
50°C
-70°C
391
397
403
409
415
MHZ


GAIN (dB)
70
50
30
10
-10
-70°C
+70°C
+50 C
-50°C
-25°C
0°C
25°C

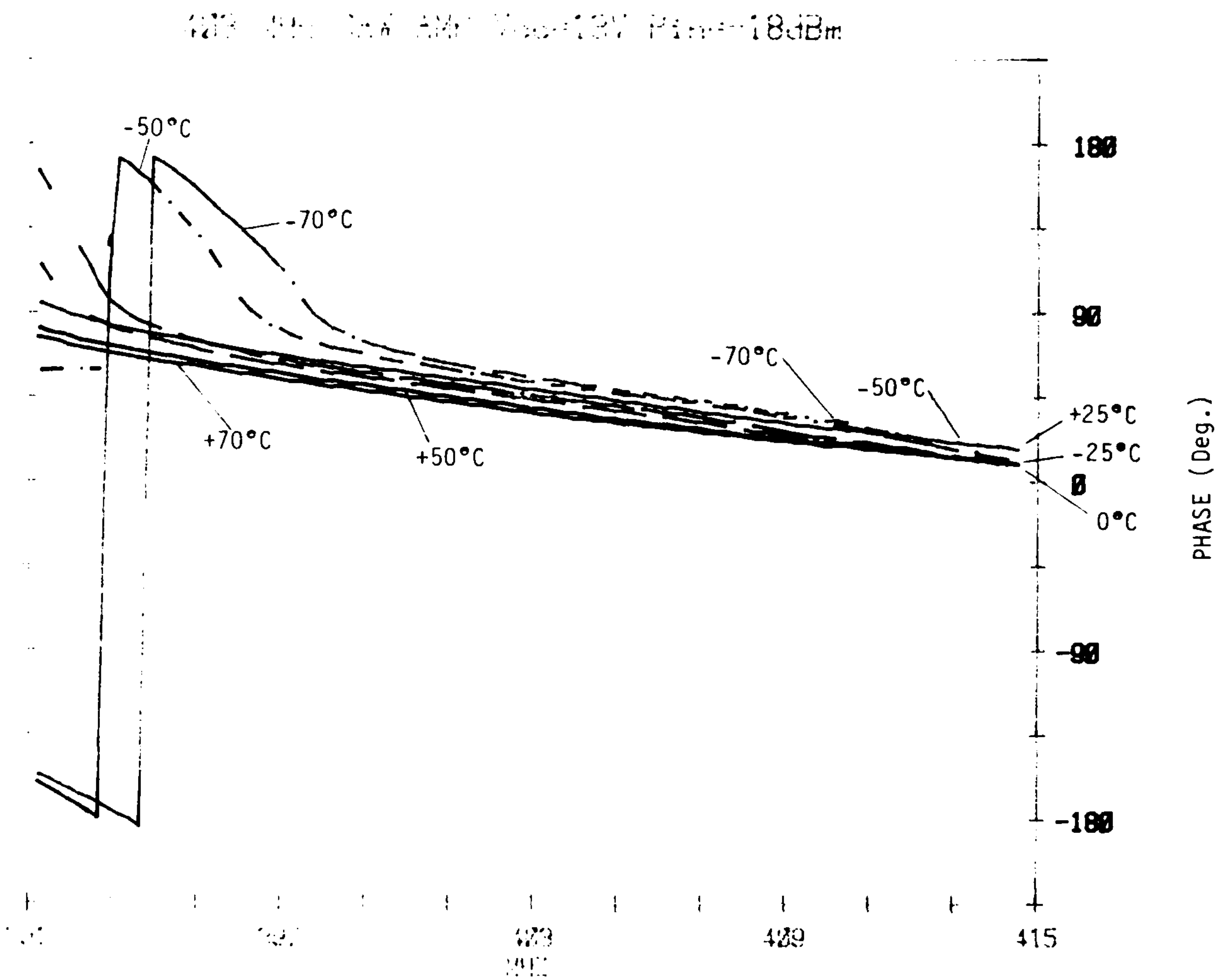

18dBm
-70°C
-50°C
+25°C
-25°C
0°C
+70°C
+50°C
180
90
0
-90
-180
PHASE (Deg.)
403
409
415


403 MHz SAW AMP
GAIN (dB)
70
50
30
10
-10
+70°C
+50°C
-50°C
-25°C
0°C
+25°C
391
397
403



PHASE (Deg.)
180
90
0
-90
-180
+25°C
-25°C
0°C
-50°C
-70°C
+50°C
+70°C
415
409

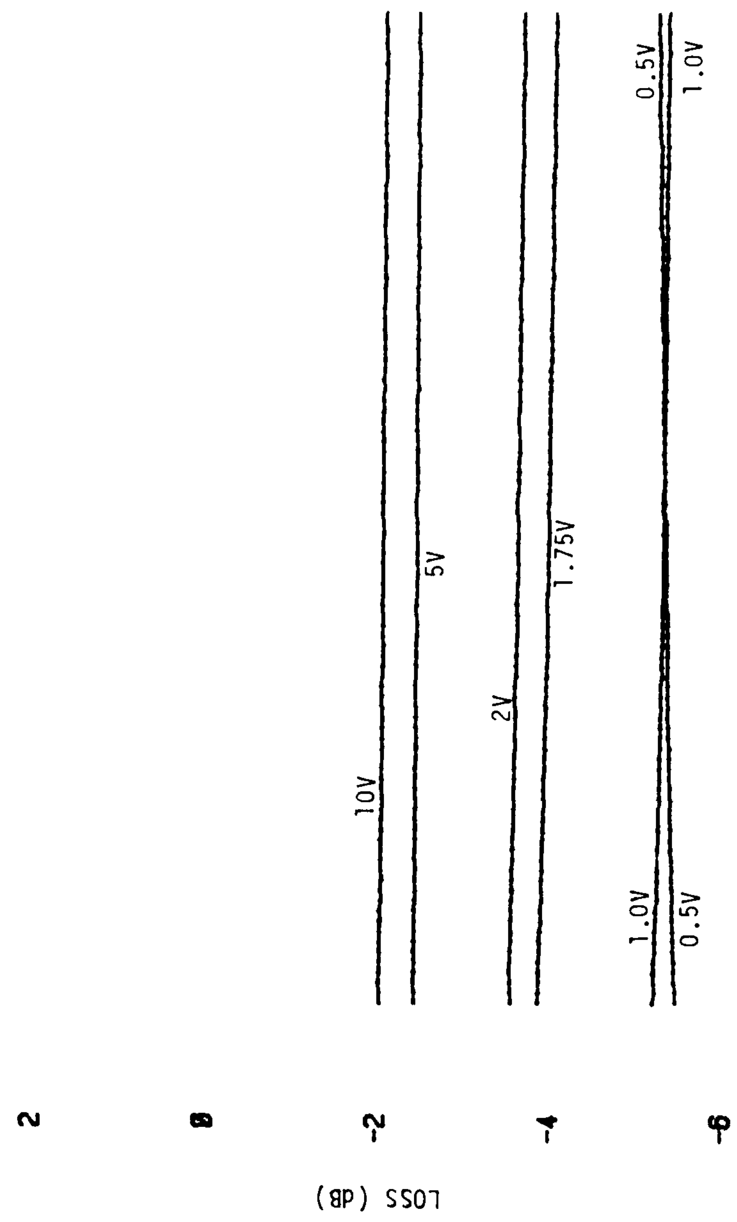

403 MH
GAIN (dB)
70
50
30
10
-10
391
397
+70°C
-50°C
-25°C
0°C
+25°C
+50°C
-50°C

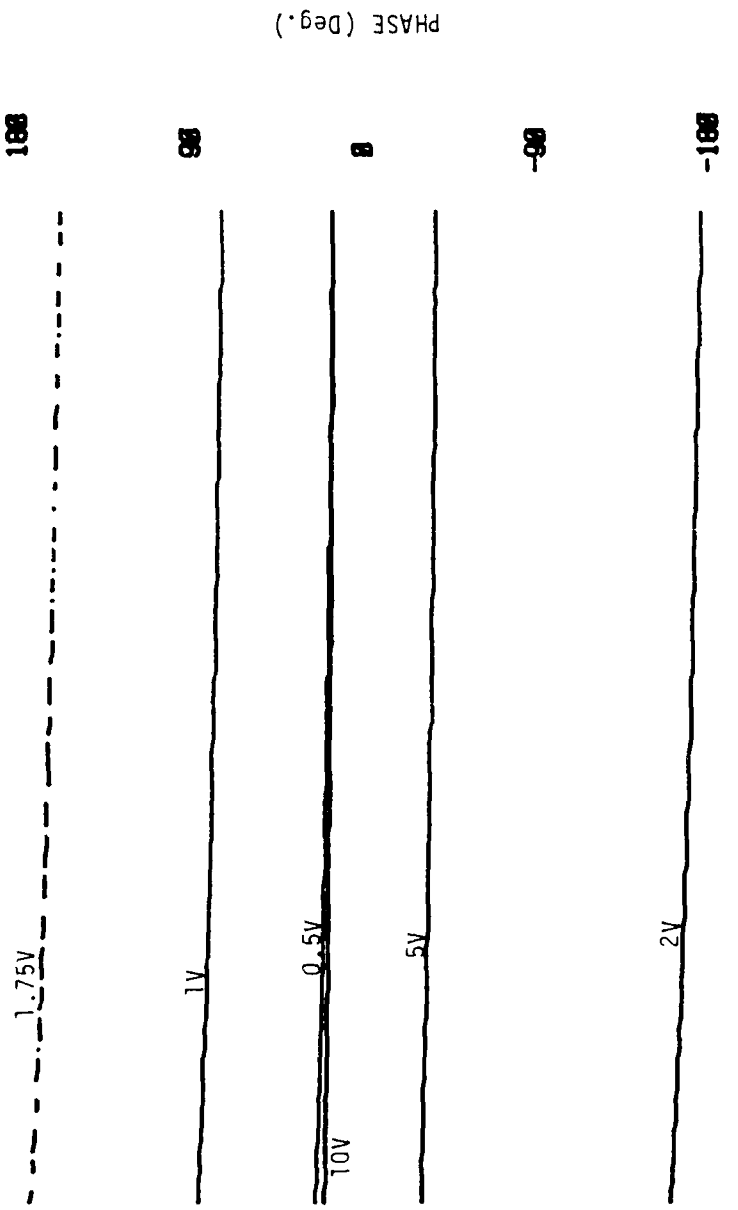


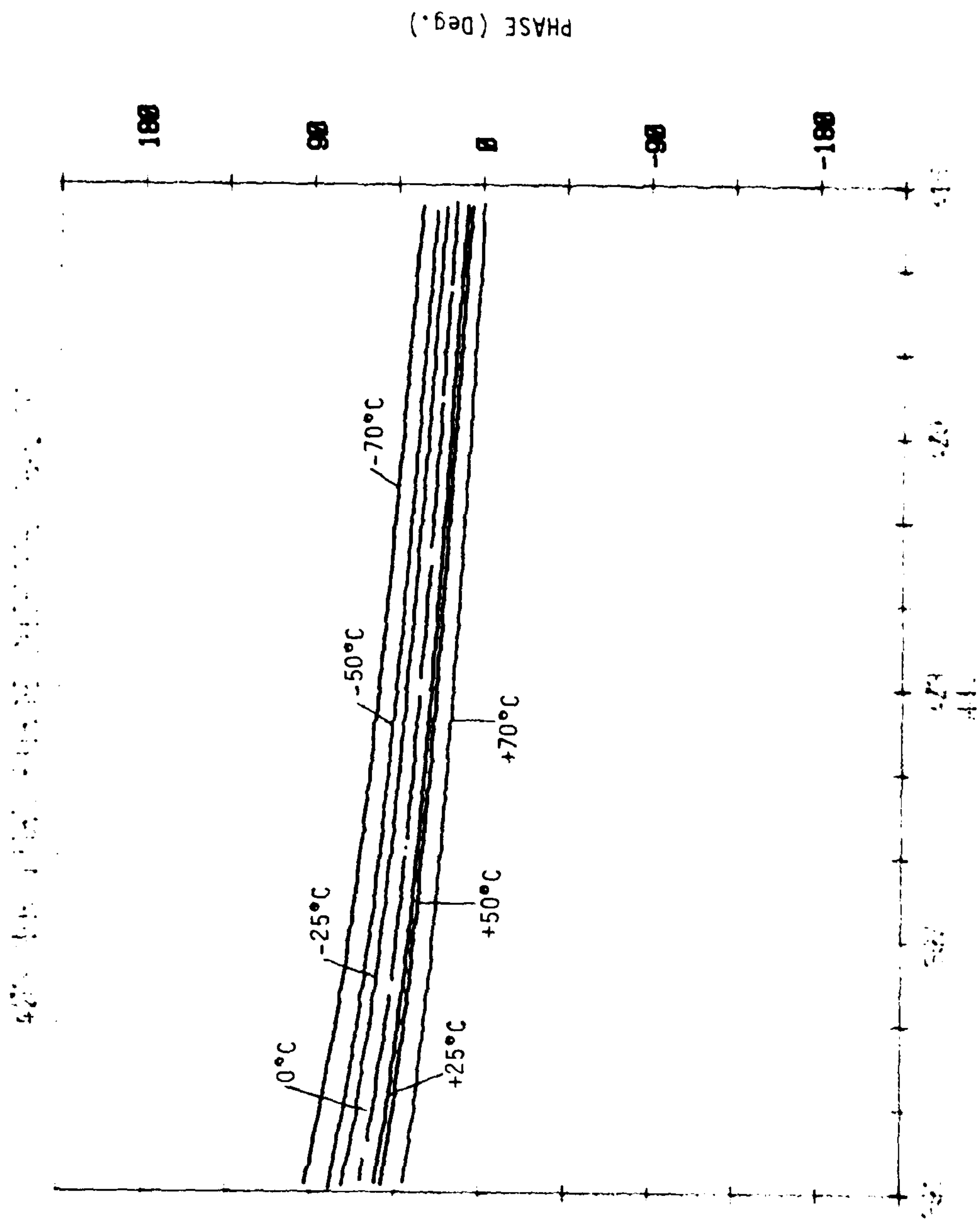
18dBm
-50°C
-70°C
-70°C
-50°C
+25°C
-25°C
0°C
+70°C
+50°C
180
90
0
-90
-180
PHASE (Deg.)
409
415

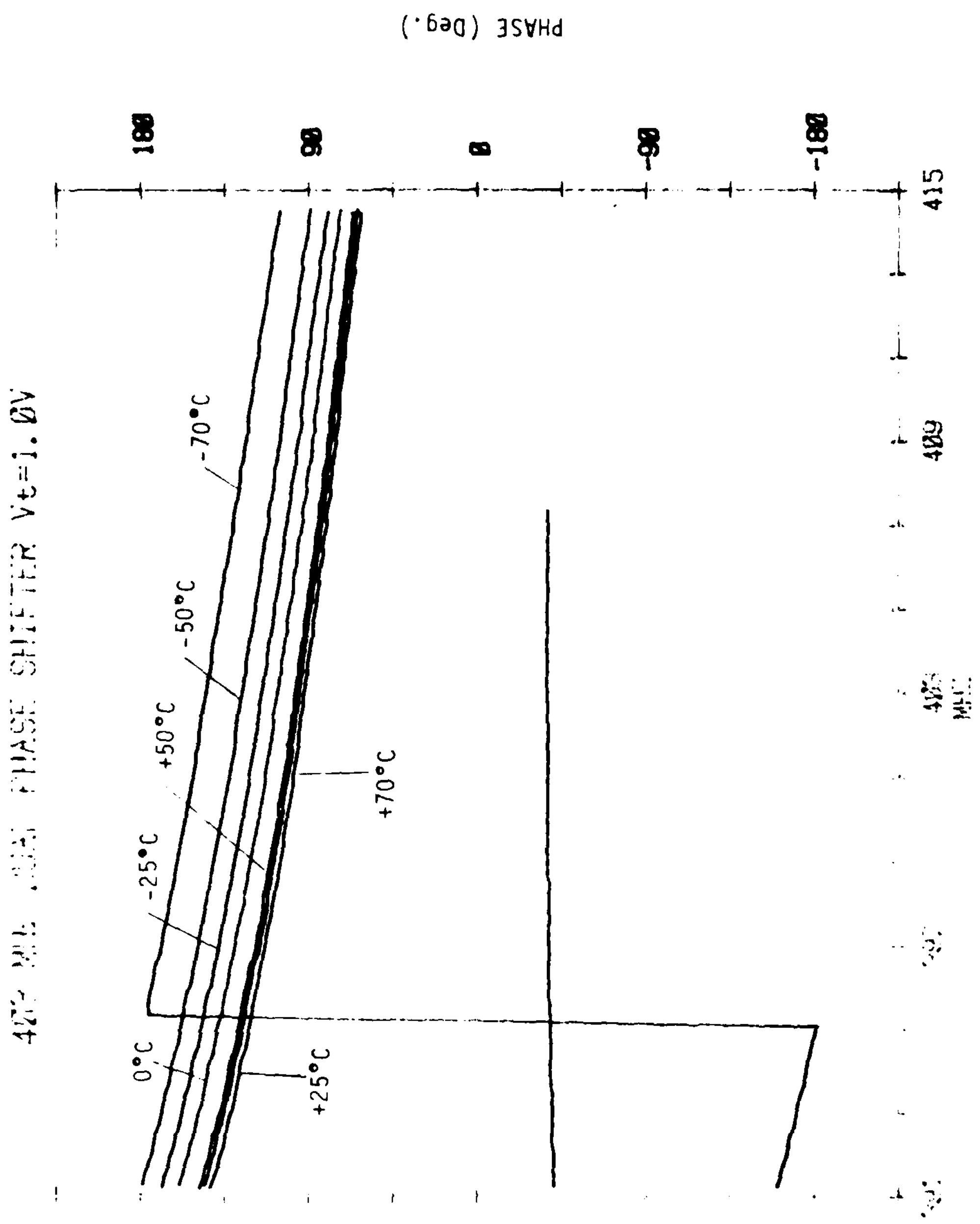
APPENDIX C

PHASE SHIFTER CHARACTERISTICS

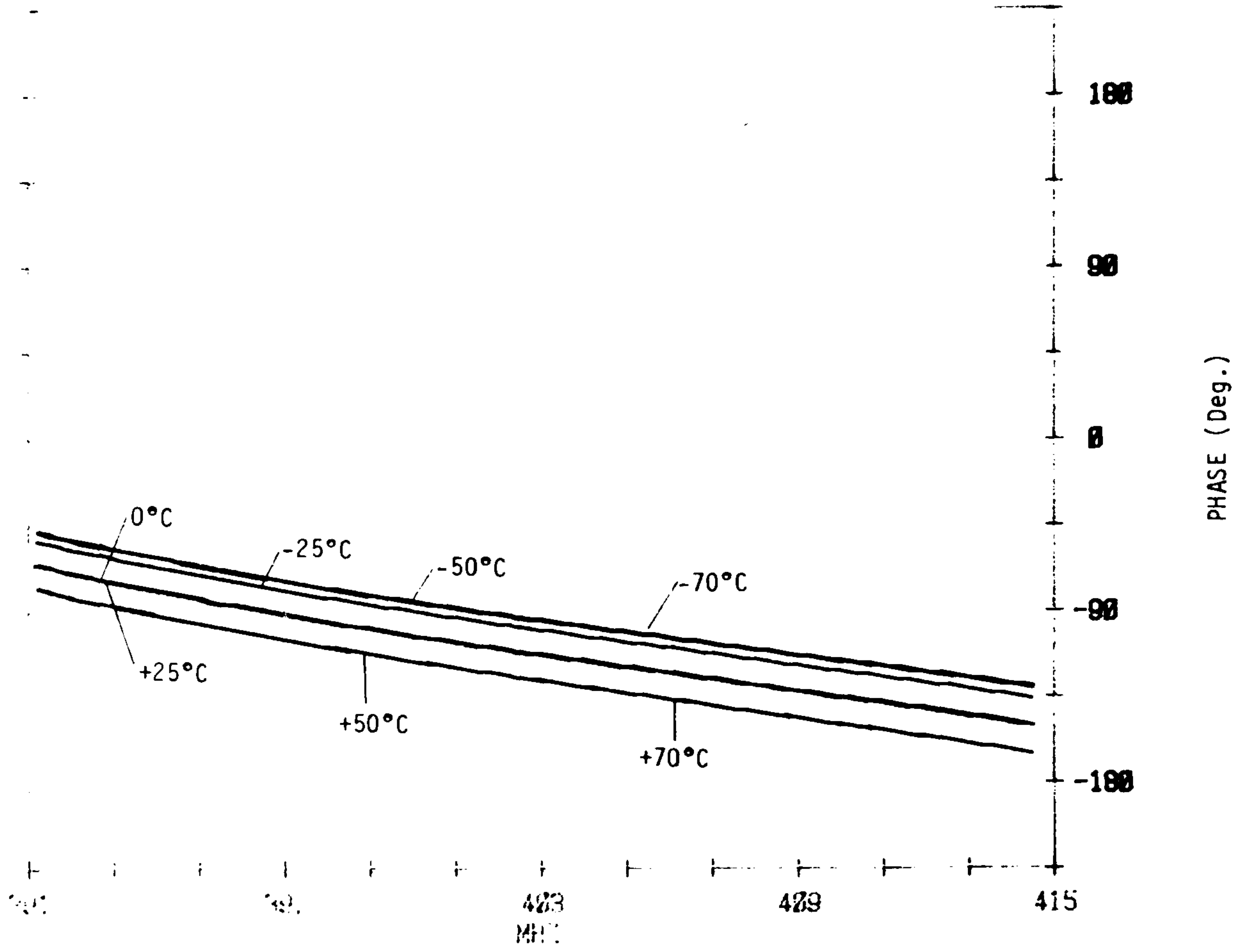

2
0
-2
-4
-6
LOSS (dB)
10V
5V
2V
1.75V
1.0V
0.5V
0.5V
1.0V


PHASE (Deg.)
180
90
0
-90
-180
1.75V
1V
0.5V
10V
5V
2V

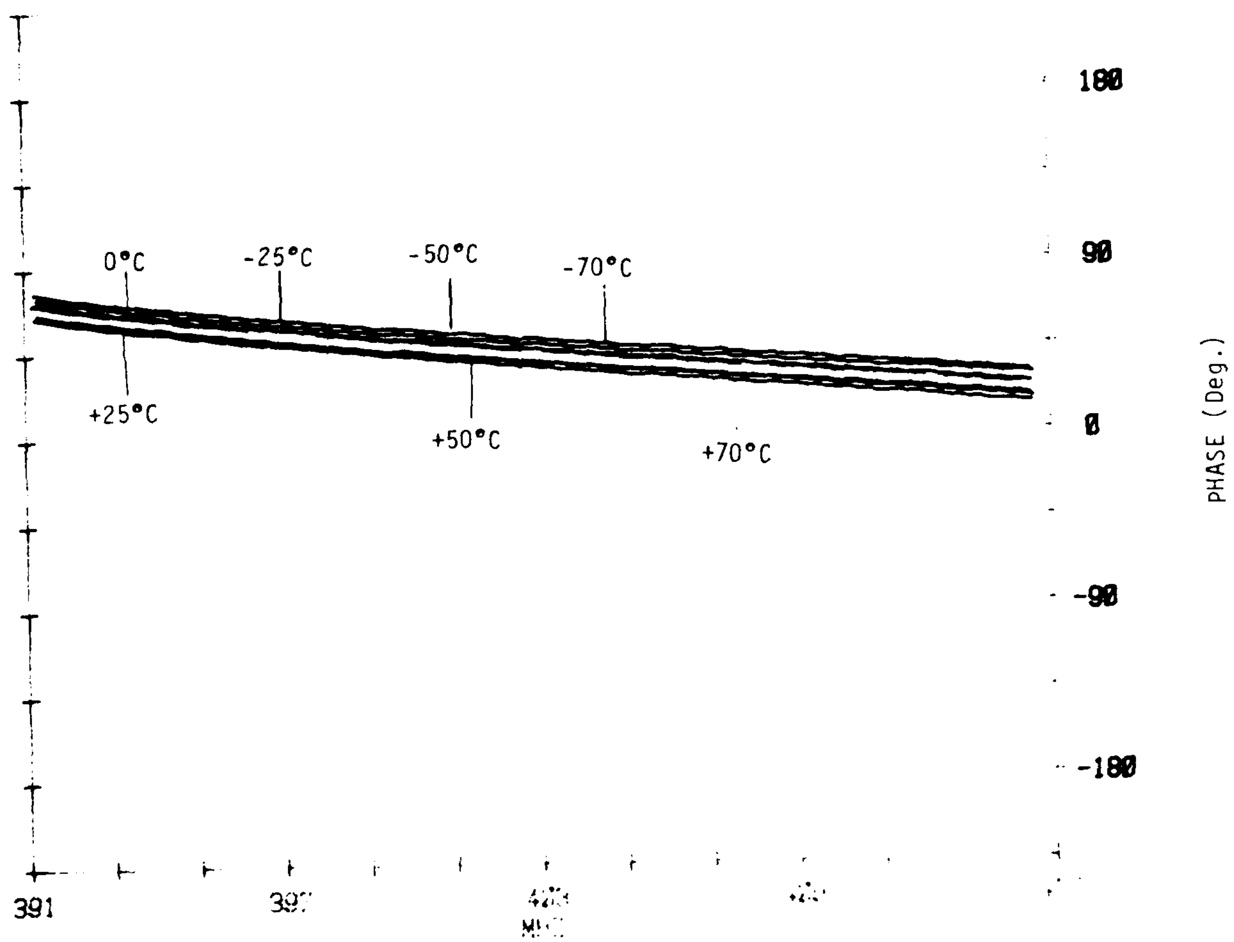

PHASE (Deg.)
180
90
0
-90
-180
-70°C
-50°C
-25°C
0°C
+25°C
+50°C
+70°C


PHASE SHIFTER Vt=1.ØV
PHASE (Deg.)
180
90
0
-90
-180
415
409
MHz
-70°C
-50°C
+50°C
-25°C
0°C
+25°C
+70°C

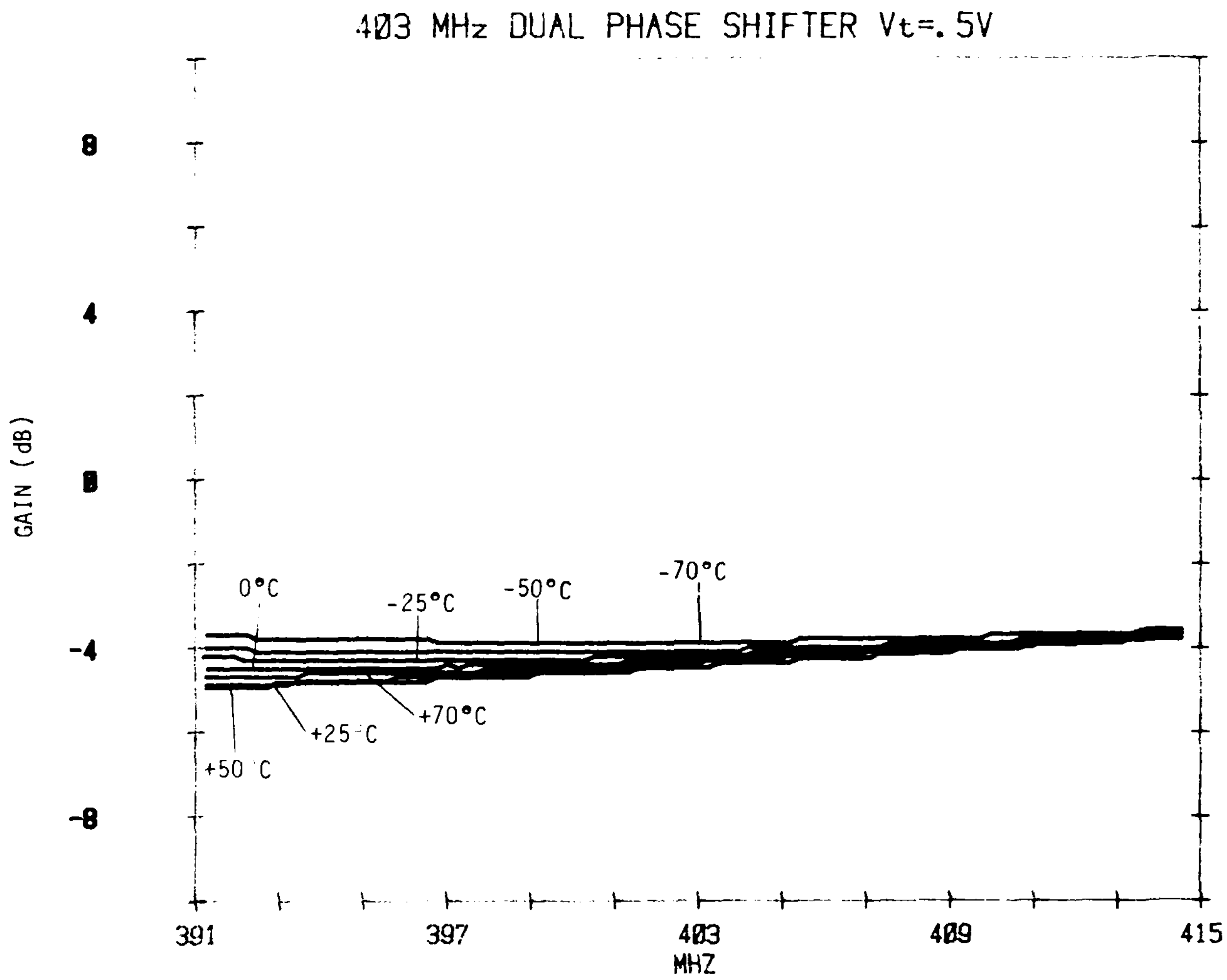
403 MHz DUAL PHASE SHIFTER Vt=2.0V



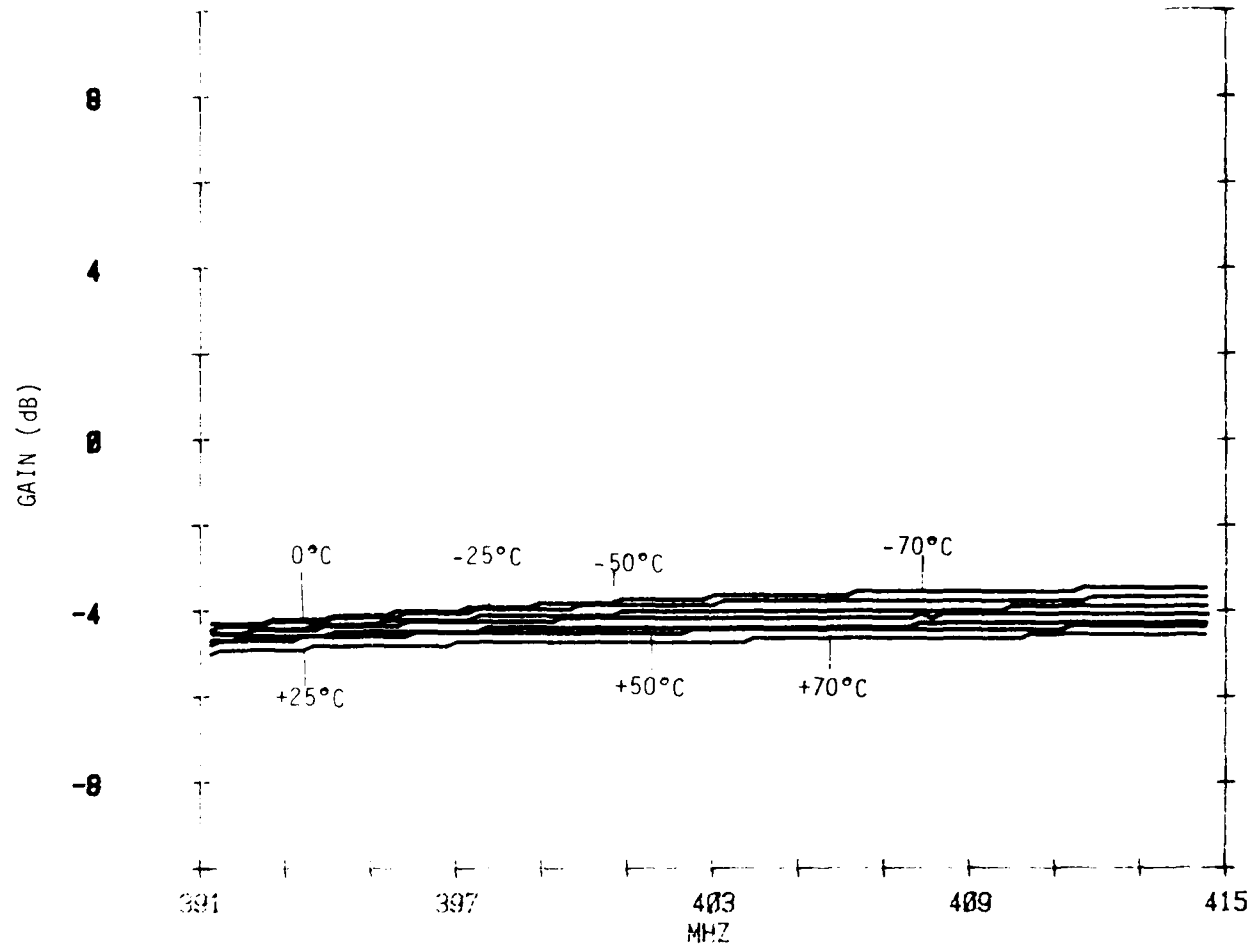
403 MHz DUAL PHASE SHIFTER



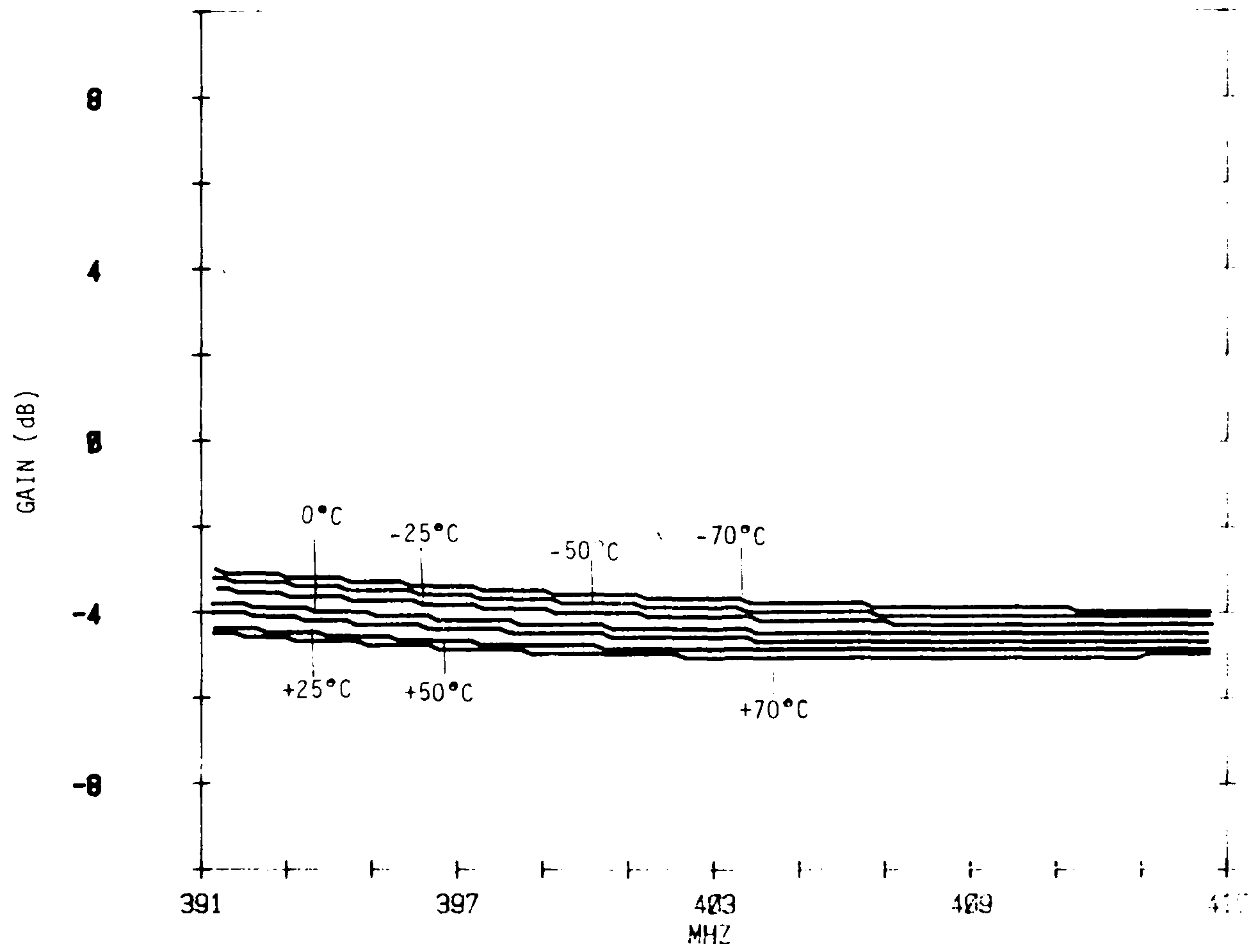

403 MHz
PHASE (Deg.)
180
90
0
-90
-180
391
0°C
+25°C
-25°C
-50°C
-70°C
+50°C


403 MHz DUAL PHASE SHIFTER Vt=.5V
GAIN (dB)
8
4
0
-4
-8
0°C
-25°C
-50°C
-70°C
+25°C
+70°C
+50°C
391
397
403
409
415
MHZ

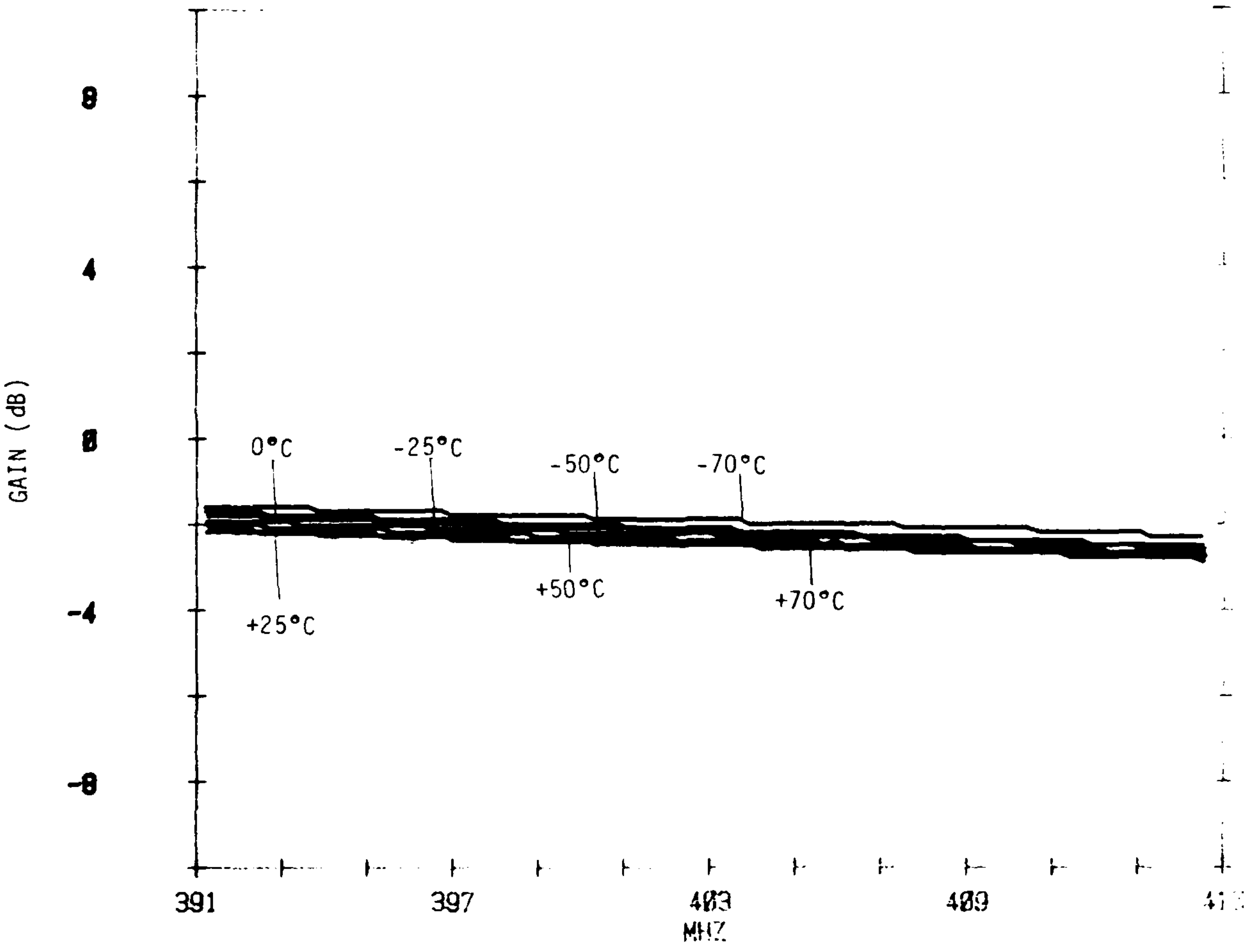
4033 MHz DUAL PHASE SHIFTER Vt=1.0V

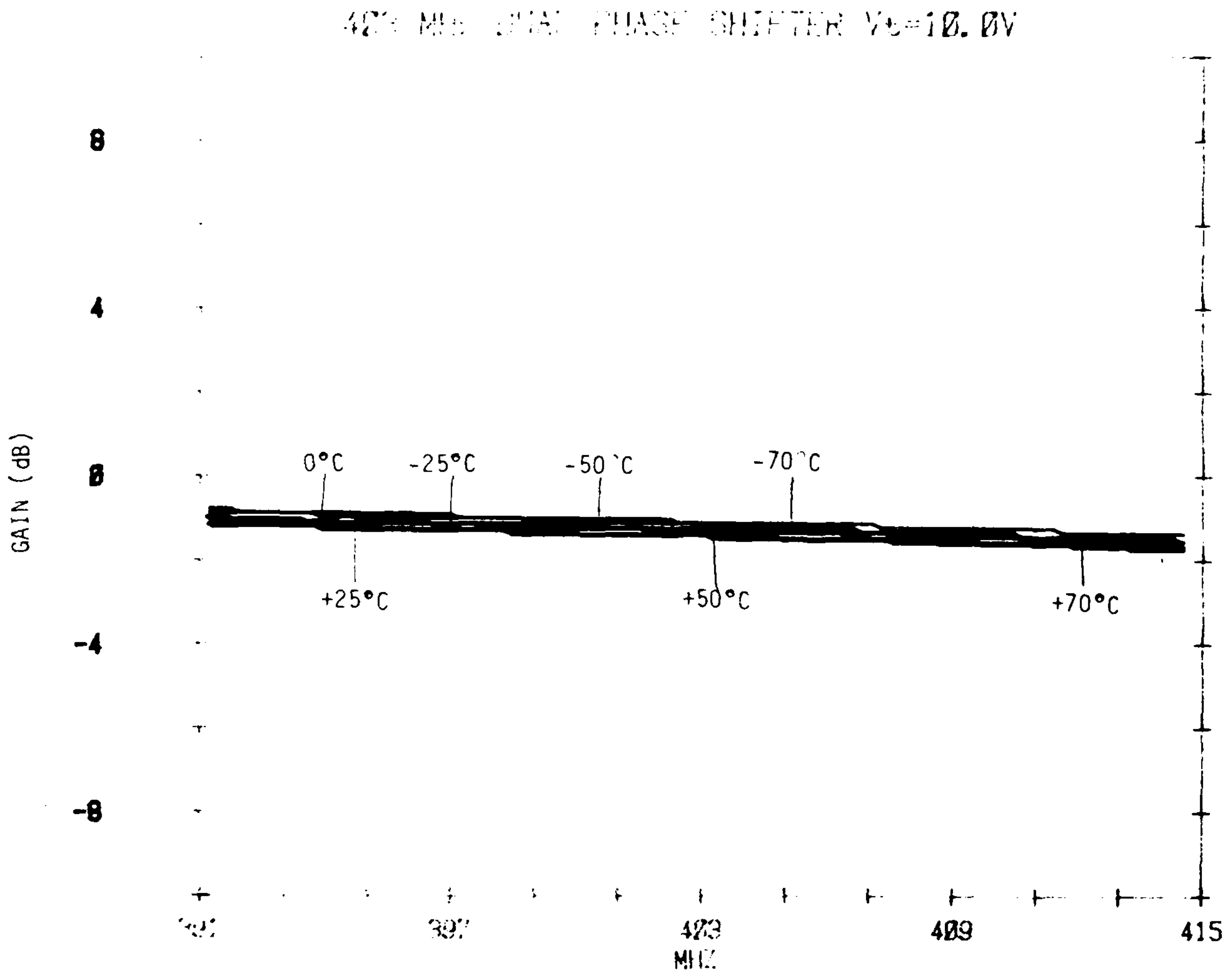


403 MHz DUAL PHASE SHIFTER Vt=2.0V



403 MHz DUAL PHASE SHIFTER V+=5.0V




PHASE SHIFTER
GAIN (dB)
8
4
0
-4
-8
0°C
-25°C
-50°C
-70°C
+25°C
+50°C
+70°C
403
409
415
MHZ

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